MG3710A
Vector Signal Generator
Operation Manual
(Standard Waveform Pattern)

Fifth Edition

- **For safety and warning information, please read this manual before attempting to use the equipment.**
- **Additional safety and warning information is provided within the MG3710A Vector Signal Generator Operation Manual (Mainframe). Please also refer to this document before using the equipment.**
- **Keep this manual with the equipment.**

ANRITSU CORPORATION

Document No.: M-W3581AE-5.0

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Symbols used in manual

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Safety Symbols Used on Equipment and in Manual

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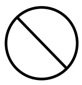
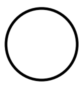


This indicates a prohibited operation. The prohibited operation is indicated symbolically in or near the barred circle.



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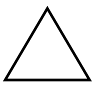

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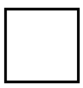
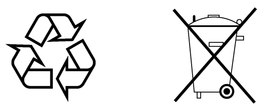


This indicates a note. The contents are described in the box.



These indicate that the marked part should be recycled.

MG3710A
Vector Signal Generator
Operation Manual (Standard Waveform Pattern)

20 January 2012 (First Edition)
31 July 2014 (Fifth Edition)

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- Adding software

  Do not download or install software that has not been specifically recommended or licensed by Anritsu.
- Network connections

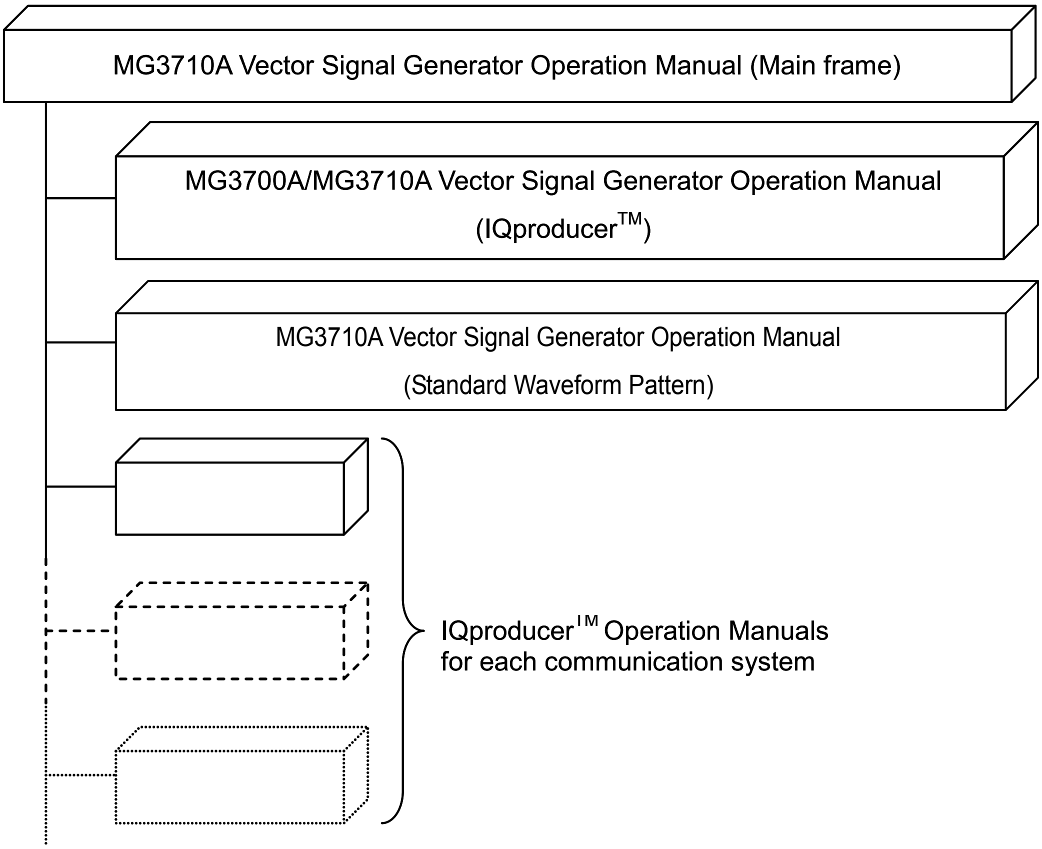
  Ensure that the network has sufficient anti-virus security protection in place.

About This Manual

■ Composition of Operation Manuals

The operation manuals for the MG3710A Vector Signal Generator are comprised as shown in the figure below.

Details on the mainframe and the software application IQproducer™ are provided in each operation manual separately. Read them when needed in addition to this manual.



■ Scope of This Manual

This manual mainly describes how to use the standard waveform patterns that can be used in the arbitrary waveform generators integrated in the MG3710A Vector Signal Generator, as well as the detailed specifications of each waveform pattern. The detailed information about the standard waveform pattern is described in Section 3 "Details of Standard Waveform Pattern." The detailed operation method of the standard waveform pattern in the MG3710A Vector Signal Generator is described in the MG3710A Operation Manual (Mainframe). Read it in addition to this manual.

Table of Contents

Chapter 1 Outline

This section provides an outline of the standard waveform pattern for the MG3710A Vector Signal Generator.

1.1 Outline of Product

The standard waveform pattern for the MG3710A Vector Signal Generator (hereafter referred to as “standard waveform pattern”) consists of waveform patterns (see Note) that are used in a wide range of applications from research and development to manufacturing of the systems, devices, and equipment in the field of digital mobile communications.

The standard waveform pattern can be used in the MG3710A Vector Signal Generator (hereafter referred to as “MG3710A”) that integrates an arbitrary waveform generator.

Note:

The waveform pattern described here indicates arbitrary waveform data used for supporting various radio communication systems that can be used by the arbitrary waveform generator integrated in the MG3710A.

The waveform pattern consists of two files: arbitrary waveform file and waveform information file. The arbitrary waveform file is a binary-format file with the extension “.wvd”. The waveform information file is a text-format file with the extension “.wvi”, used to control arbitrary waveform data and set the hardware for waveform data output.

Waveform patterns that use two memories as shown below can be operated easily by using a combination file that defines a combination of two waveform patterns to be loaded from memories A and B, and sets the output level for memories.

- A waveform pattern that uses two memories to output one signal, such as a W-CDMA downlink desired signal
- A waveform pattern that is generated by adding two signals, such as a desired wave used for receiver evaluation and an interference signal or AWGN, using the baseband

To use the combined waveform patterns of Memory A and B, the Combination of Baseband Signal for 1st RF/2nd RF option (MG3710A-048/148/078/178) is required.

Chapter 2 How to Use Standard Waveform Pattern

This chapter describes how to use the standard waveform pattern and the configuration of the standard waveform pattern package.

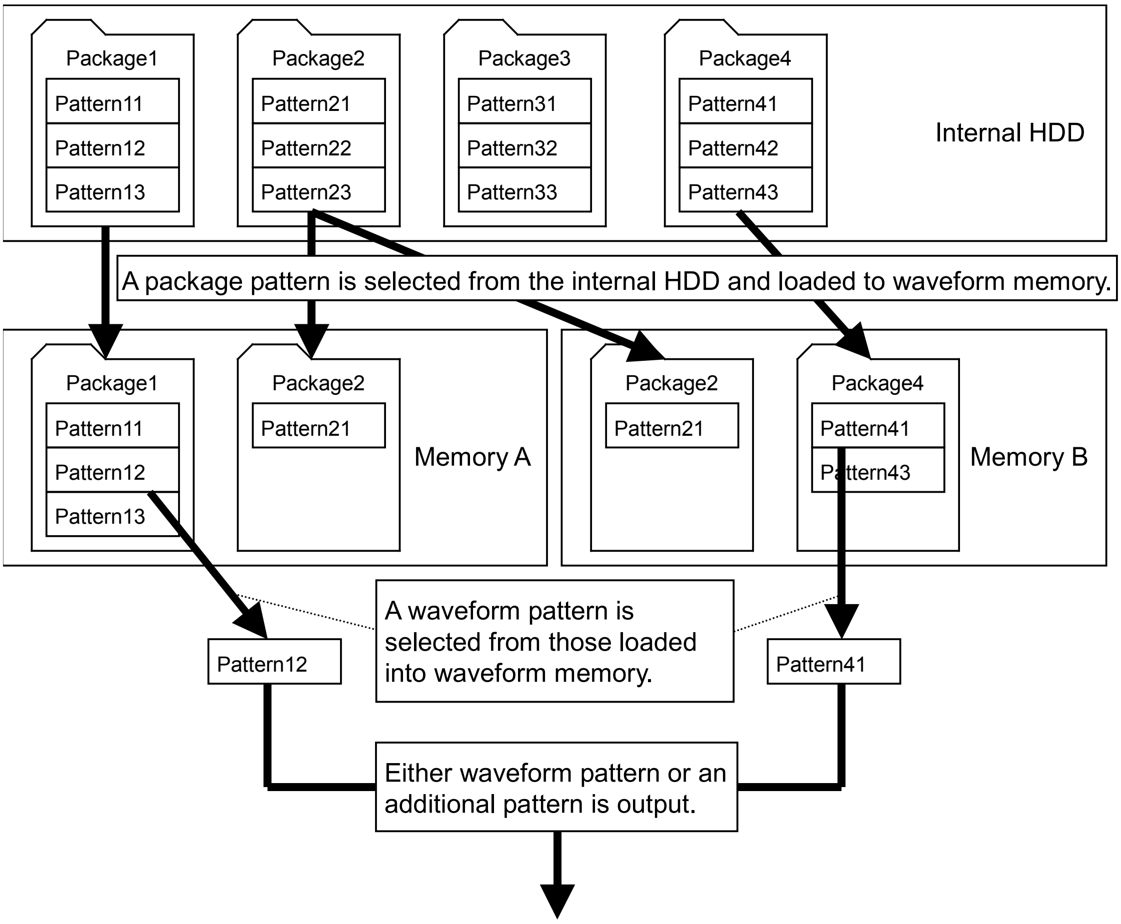
2.1 How to Use Standard Waveform Pattern

The standard waveform pattern is shipped being stored in the internal hard disk of the MG3710A.

The waveform pattern stored in the internal hard disk is reproduced by the arbitrary waveform generator integrated in the MG3710A, and used to perform vector modulation.

The waveform patterns are classified by communication type and stored in a folder. This folder is called as a package, and the standard waveform patterns classified by communication type are stored in each package with the corresponding communication system name. When reproducing a waveform pattern, it is necessary first to load the package pattern stored in the internal hard disk to a waveform memory in the MG3710A. If the Combination of Baseband Signal for 1st RF/2nd RF option is installed, it is possible to have two types of I/Q 2-channel configuration waveform memory. One of the two or both of memories can be loaded to a waveform memory in the MG3710A.

Then, select a waveform pattern to be output from the patterns loaded into the waveform memory. Only one waveform pattern can be selected from each memory. A waveform pattern selected from the waveform memory A or B, or an additional waveform generated by adding two waveform patterns selected from both waveform memories A and B is output.



For details on how to select waveform pattern, refer to 7.3 “Baseband Mode” in *MG3710A Vector Signal Generator Operation Manual (Mainframe)*.

2.2 Configuration of Standard Waveform Pattern Package

The standard waveform patterns are stored in the internal hard disk of the MG3710A, classified into the packages with the corresponding communication system name.

Table 2.2-1 List of packages

Package name	Contents
W-CDMA (BS Rx test)	Waveform patterns for 3GPP W-CDMA, BS Rx test
W-CDMA (BS Tx test)	Waveform patterns for 3GPP W-CDMA, BS Tx test
W-CDMA_A (UE Rx test)	Waveform patterns for 3GPP W-CDMA, UE Rx test used in waveform memory A
W-CDMA_B (UE Rx test)	Waveform patterns for 3GPP W-CDMA, UE Rx test used in waveform memory B
W-CDMA (UE Rx test)	A combination file that defines a combination of two waveform patterns W-CDMA_A (UE Rx Test) and W-CDMA_B (UE Rx Test)
W-CDMA (UE Tx test)	Waveform patterns for 3GPP W-CDMA, UE Tx test
W-CDMA_CMB	A combination file that defines a combination of a W-CDMA desired wave and an interference signal or AWGN
LTE_FDD (BS Tx test)	Waveform patterns for 3GPP LTE (FDD), BS Tx test
LTE_TDD (BS Tx test)	Waveform patterns for 3GPP LTE (TDD), BS Tx test
PDC	Various waveform patterns for PDC
PDC_CMB	A combination file that defines a combination of a PCC desired wave and an interference signal
PHS	Various waveform patterns for PHS
PHS_CMB	A combination file that defines a combination of a PHS desired wave and an interference signal
GSM	Various waveform patterns for GSM
CDMA2000	Various waveform patterns for CDMA2000 1X
CDMA2000_1xEV-DO	Various waveform patterns for CDMA2000 1xEV-DO
WLAN	Various waveform patterns for IEEE802. 11a/b/g
Digital_Broadcast	Waveform patterns for the Digital Broadcast
Bluetooth	Various waveform patterns for Bluetooth
GPS	Various waveform patterns for GPS
MobileWiMAX	Waveform patterns for Mobile WiMAX, BS Tx device test
Tone	Tone Signal Waveform Pattern
PhaseCoherence	Waveform Pattern for MG3710A phase adjustment

Chapter 3 Details of Standard Waveform Pattern

This section describes each standard waveform pattern in detail.

Note :

In order to add AWGN to the standard waveform pattern, your MG3710A must be equipped with AWGN option. For details on how to add AWGN, refer to 7.5 “AWGN” in MG3710A Vector Signal Generator Operation Manual (Mainframe).

3.1 W-CDMA Waveform Pattern

Table 3.1-1 lists the W-CDMA waveform patterns.

Table 3.1-1 List of W-CDMA waveform patterns (1/4)

Waveform Pattern Name	UL/DL	Channel Configuration	3GPP Reference Standard	Main Application
Package name: W-CDMA (BS Rx test)				
UL_RMC_12_2kbps*1	UL	DPCCH, DPDCH	TS25.141 A.2	BS RX test
UL_RMC_12_2kbps_ACS*2	UL	DPCCH, DPDCH	TS25.141 A.2	BS RX test
UL_RMC_64kbps*2	UL	DPCCH, DPDCH	TS25.141 A.3	BS RX test
UL_RMC_144kbps*2	UL	DPCCH, DPDCH	TS25.141 A.4	BS RX test
UL_RMC_384kbps*2	UL	DPCCH, DPDCH	TS25.141 A.5	BS RX test
UL_AMR_TFCS1*1	UL	DPCCH, DPDCH	TS25.944 4.1.2	BS RX test
UL_AMR_TFCS2*1	UL	DPCCH, DPDCH	TS25.944 4.1.2	BS RX test
UL_AMR_TFCS3*1	UL	DPCCH, DPDCH	TS25.944 4.1.2	BS RX test
UL_ISDN*2	UL	DPCCH, DPDCH	TS25.944 4.1.2	BS RX test
UL_64kbps_Packet*1	UL	DPCCH, DPDCH	TS25.944 4.1.2	BS RX test
UL_Interferer	UL	DPCCH, DPDCH	TS25.141 I	BS RX test
UL_Interferer_ov3*3	UL	DPCCH, DPDCH	TS25.141 I	BS RX test
Package name: W-CDMA (BS Tx test)				
TestModel_1_4DPCH	DL	P-CPICH, P-CCPCH, SCH,PICH, S-CCPCH,4 DPCH	TS25.141 V11.4.0	BS TX device test
TestModel_1_8DPCH	DL	P-CPICH, P-CCPCH, SCH,PICH, S-CCPCH,8 DPCH	TS25.141 V11.4.0	BS TX device test
TestModel_1_16DPCH	DL	P-CPICH, P-CCPCH, SCH, PICH, S-CCPCH, 16 DPCH	TS25.141 V11.4.0	BS TX device test
TestModel_1_32DPCH	DL	P-CPICH, P-CCPCH, SCH, PICH, S-CCPCH, 32 DPCH	TS25.141 V11.4.0	BS_Tx device test
TestModel_1_64DPCH	DL	P-CPICH, P-CCPCH, SCH, PICH, S-CCPCH, 64 DPCH	TS25.141 V11.4.0	BS TX device test
TestModel_2	DL	P-CPICH, P-CCPCH, SCH, PICH, S-CCPCH, 3 DPCH	TS25.141 V11.4.0	BS TX device test
TestModel_3_4DPCH	DL	P-CPICH, P-CCPCH, SCH,PICH, S-CCPCH,4 DPCH	TS25.141 V11.4.0	BS TX device test
TestModel_3_8DPCH	DL	P-CPICH, P-CCPCH, SCH,PICH, S-CCPCH,8 DPCH	TS25.141 V11.4.0	BS TX device test

Table 3.1-1 List of W-CDMA waveform patterns (2/4)

Waveform Pattern Name	UL/DL	Channel Configuration	3GPP Reference Standard	Main Application
TestModel_3_16DPCH	DL	P-CPICH, P-CCPCH, SCH, PICH, S-CCPCH, 16 DPCH	TS25.141 V11.4.0	BS TX device test
TestModel_3_32DPCH	DL	P-CPICH, P-CCPCH, SCH, PICH, S-CCPCH, 32 DPCH	TS25.141 V11.4.0	BS TX device test
TestModel_4	DL	P-CCPCH, SCH	TS25.141 V11.4.0	BS TX device test
TestModel_4_CPICH	DL	P-CPICH,P-CCPCH, SCH	TS25.141 V11.4.0	BS TX device test
TestModel_ 1_64DPCHx2*5	DL	P-CPICH, P-CCPCH, SCH, PICH, S-CCPCH, 64 DPCH	TS25.141 V11.4.0	BS TX device test
TestModel_ 1_64x2_10M*5, *6	DL	P-CPICH, P-CCPCH, SCH, PICH, S-CCPCH, 64 DPCH	TS25.141 V11.4.0	BS TX device test
TestModel_ 1_64x2_15M*5, *6	DL	P-CPICH, P-CCPCH, SCH, PICH, S-CCPCH, 64 DPCH	TS25.141 V11.4.0	BS TX device test
TestModel_ 1_64DPCHx3*6	DL	P-CPICH, P-CCPCH, SCH, PICH, S-CCPCH, 64 DPCH	TS25.141 V11.4.0	BS TX device test
TestModel_ 1_64DPCHx4*5	DL	P-CPICH, P-CCPCH, SCH, PICH, S-CCPCH, 64 DPCH	TS25.141 V11.4.0	BS TX device test
TestModel_5_4DPCH	DL	P-CPICH,P-CCPCH, SCH,PICH, S-CCPCH, 4 DPCH,HS-SCCH, 4 HS-PDSCH	TS25.141 V11.4.0	BS TX device test
TestModel_5_2HSPDSCH	DL	P-CPICH, P-CCPCH, SCH, PICH, S-CCPCH, 6 DPCH, HS-SCCH, 2 HS-PDSCH	TS25.141 V11.4.0	BS TX device test
TestModel_5_4HSPDSCH	DL	P-CPICH, P-CCPCH, SCH, PICH, S-CCPCH, 14 DPCH, HS-SCCH, 4 HS-PDSCH	TS25.141 V11.4.0	BS TX device test
TestModel_5_8HSPDSCH	DL	P-CPICH, P-CCPCH, SCH, PICH, S-CCPCH, 30 DPCH, HS-SCCH, 8 HS-PDSCH	TS25.141 V11.4.0	BS TX device test

Table 3.1-1 List of W-CDMA waveform patterns (3/4)

Waveform Pattern Name	UL/DL	Channel Configuration	3GPP Reference Standard	Main Application
TestModel_6_4HSPDSCH	DL	P-CPICH,P-CCPCH, SCH,PICH, S-CCPCH,14 DPCH,HS-SCCH, 4 HS-PDSCH	TS25.141 V11.4.0	BS TX device test
TestModel_6_8HSPDSCH	DL	P-CPICH, P-CCPCH, SCH, PICH, S-CCPCH, 30 DPCH, HS-SCCH, 8 HS-PDSCH	TS25.141 V11.4.0	BS TX device test
Package name: W-CDMA_A (UE Rx test)				
DL_CPICH	DL	P-CPICH	-	UE RX test
P-CCPCH*3	DL	P-CCPCH	TS25.944 4.1.1*4	UE RX test
DL_RMC_12_2kbps_ACS*2	DL	P-CPICH, P-CCPCH, SCH, PICH, DPCH	TS25.101 A.3.1 TS25.101 C.3.1	UE RX test
DL_Interferer	DL	P-CPICH, P-CCPCH, SCH, PICH, OCNS	TS25.101 C.4	UE RX test
DL_Interferer_ov3*7	DL	P-CPICH, P-CCPCH, SCH, PICH, OCNS	TS25.101 C.4	UE RX test
Package name: W-CDMA_B (UE Rx test)				
DL_RMC_12_2kbps_RX*3	DL	P-CPICH, SCH, PICH, DPCH	TS25.101 A.3.1 TS25.101 C.3.1	UE RX test
DL_RMC_12_2kbps*3	DL	P-CPICH, SCH, PICH, DPCH, OCNS	TS25.101 A.3.1 TS25.101 C.3.2	UE RX test
DL_RMC_12_2kbps_MIL*3	DL	P-CPICH, SCH, PICH, DPCH, OCNS	TS25.101 A.3.1 TS25.101 C.3.1	UE RX test
DL_RMC_64kbps*3	DL	P-CPICH, SCH, PICH, DPCH, OCNS	TS25.101 A.3.2 TS25.101 C.3.2	UE RX test
DL_RMC_144kbps*3	DL	P-CPICH, SCH, PICH, DPCH, OCNS	TS25.101 A.3.3 TS25.101 C.3.2	UE RX test
DL_RMC_384kbps*3	DL	P-CPICH, SCH, PICH, DPCH, OCNS	TS25.101 A.3.4 TS25.101 C.3.2	UE RX test
DL_AMR_TFCS1*3	DL	P-CPICH, SCH, PICH, DPCH, OCNS	TS25.944 4.1.1.3 TS25.101 C.3.2	UE RX test
DL_AMR_TFCS2*3	DL	P-CPICH, SCH, PICH, DPCH, OCNS	TS25.944 4.1.1.3 TS25.101 C.3.2	UE RX test
DL_AMR_TFCS3*3	DL	P-CPICH, SCH, PICH, DPCH, OCNS	TS25.944 4.1.1.3 TS25.101 C.3.2	UE RX test
DL_ISDN*1, *3	DL	P-CPICH, SCH, PICH, DPCH, OCNS	TS25.944 4.1.1.3 TS25.101 C.3.2	UE RX test

Table 3.1-1 List of W-CDMA waveform patterns (4/4)

Waveform Pattern Name	UL/DL	Channel Configuration	3GPP Reference Standard	Main Application
DL_384kbps_Packet*3	DL	P-CPICH, SCH, PICH, DPCH, OCNS	TS25.944 4.1.1.3 TS25.101 C.3.2	UE RX test
DL_Interferer	DL	P-CPICH, P-CCPCH, SCH, PICH, OCNS	TS25.101 C.4	UE RX test
DL_Interferer_ov3*7	DL	P-CPICH, P-CCPCH, SCH, PICH, OCNS	TS25.101 C.4	UE RX test
Package name: W-CDMA (UE Tx test)				
UL_RMC_12_2kbps_TX*2	UL	DPCCH, DPDCH	TS25.101 A.2.1	UE TX device test

*1: To use this waveform pattern, Combination of Baseband Signal (option), ARB Memory Upgrade 256 Msample (option), or ARB Memory Upgrade 1024 Msample (option), is required.

*2: To use this waveform pattern, ARB Memory Upgrade 256 Msample (option) or ARB Memory Upgrade 1024 Msample (option), is required.

*3: Since waveform patterns (excluding DL_RMC12_2kbps_ACS) for the UE RX test do not include P-CCPCH, they must be used in combination with a P-CCPCH waveform pattern. Refer Table 3.1-2 for the combination files in which these combinations are defined.

*4: An 11-bit SFN is added to the head of each BCH Transport block.

*5: x2, x3, and x4 indicate the number of multicarriers 2, 3, and 4, respectively.

*6: 10M and 15M indicate the frequency spacing values of the multi-carrier.

*7: When the Combination of Baseband Signal option is installed in MG3710A, select a waveform pattern generated using the W-CDMA waveform pattern generation function of the MG3710A IQproducer or by the MX370101A HSDPA IQproducer (only the waveform patterns that can be configured using only one memory) for memory A on the MG3710A while selecting this pattern for memory B to output a signal that is generated by adding the desired signal and the interference signal using baseband.

For a downlink W-CDMA desired signal, which is configured using two memories, transfer and selection of waveform patterns can be operated easily by selecting a combination file listed in Table 3.1-2 below when the MG3710A is in the Defined mode.

Table 3.1-2 List of combination files for W-CDMA desired signal

Combination File Name	Comment
Package name: W-CDMA (UE Rx test)	
DL_CMB_RMC_12_2k_RX	Downlink Reference Measurement Channel (12.2 kbps) for RX test except "Maximum Input Level" Scrambling Code = 80h DTCH information data = PN9
DL_CMB_RMC_12_2k	Downlink Reference Measurement Channel (12.2 kbps) for Performance test Scrambling Code = 80h DTCH information data = PN9
DL_CMB_RMC_12_2k_MIL	Downlink Reference Measurement Channel (12.2 kbps) for "Maximum Input Level" Scrambling Code = 80h DTCH information data = PN9
DL_CMB_RMC_64k	Downlink Reference Measurement Channel (64 kbps) for Performance test Scrambling Code = 80h DTCH information data = PN9
DL_CMB_RMC_144k	Downlink Reference Measurement Channel (144 kbps) for Performance test Scrambling Code = 80h DTCH information data = PN9
DL_CMB_RMC_384k	Downlink Reference Measurement Channel (384 kbps) for Performance test Scrambling Code = 80h DTCH information data = PN9
DL_CMB_AMR_TFCS1	Downlink AMR for TFCS1 Scrambling Code = 80h DTCH information data = PN9
DL_CMB_AMR_TFCS2	Downlink AMR for TFCS2 Scrambling Code = 80h DTCH information data = PN9
DL_CMB_AMR_TFCS3	Downlink AMR for TFCS3 Scrambling Code = 80h DTCH information data = PN9
DL_CMB_ISDN	Downlink ISDN Scrambling Code = 80h DTCH information data = PN9
DL_CMB_384k_Packet	Downlink 384 kbps Packet Scrambling Code = 80h DTCH information data = PN9

***Note*:**

To use this combination file, Combination of Baseband Signal (option) is required.

Transfer and selection of an additional waveform pattern that is generated by adding two signals, such as a desired signal + an interference signal or a desired signal + AWGN, and using two memories, can be operated easily by selecting a combination file listed in Table 3.1-3 below when the MG3710A is in the Defined mode.
Although combinations of uplink signals for BS reception evaluation are provided as standard, it is also possible to combine downlink signals by using the W-CDMA IQproducer and its Combination File Edit function. In this event, it is necessary to set the scrambling code and channelization code in accordance with the actual operating conditions.

Table 3.1-3 List of combination files for W-CDMA BS reception test

Combination File Name	Comment
Package name: W-CDMA_CMB	
WCDMA_BS_ACS*1	For TS25.141 Adjacent Channel Selectivity test UL_RMC12_2kbps + UL_Interferer (5 MHz offset)
WCDMA_BS_DRange*2	For TS25.141 Dynamic Range test UL_RMC12_2kbps + AWGN

*1: To use this combination file, Combination of Baseband Signal (option), ARB Memory Upgrade 256 Msample (option), or ARB Memory Upgrade 1024 Msample (option), is required.

*2: To use this combination file, AWGN (option), ARB Memory Upgrade 256 Msample (option), or ARB Memory Upgrade 1024 Msample (option), is required.

3.1.1 UL_RMCxxxkbps

These waveform patterns execute channel coding, division and spreading to physical channels, and power setting conforming to the UL Reference Measurement Channel standard described in 3GPP TS 25.141 Annex A.

Table 3.1.1-1 lists the parameters commonly used by each waveform pattern. When outputting each waveform pattern, marker signal (Marker 1, Marker 2) as outlined in the Table 3.1.1-1 is output from Marker1 Output connector of MG3710A rear panel or from AUX connector. For details of output connector setting, refer to 7.4.2 "Route Output Connectors" in *MG3710A Vector Signal Generator Operation Manual (Mainframe)*.

Table 3.1.1-1 List of common parameters

Marker Signal	Generating SG	Waveform Memory	Signal Name
Marker1	SG1	Memory A	SG1 Marker1 A
		Memory B	SG1 Marker1 B
	SG2	Memory A	SG2 Marker1 A
		Memory B	SG2 Marker1 B
Marker2	SG1	Memory A	SG1 Marker2 A
		Memory B	SG1 Marker2 B
	SG2	Memory A	SG2 Marker2 A
		Memory B	SG2 Marker2 B
Marker3	SG1	Memory A	SG1 Marker3 A
		Memory B	SG1 Marker3 B
	SG2	Memory A	SG2 Marker3 A
		Memory B	SG2 Marker3 B

♦ Channel coding parameters for UL_RMC_12_2kbps and UL_RMC_12_2kbps_ACS

Table 3.1.1-2 Physical channel parameters for UL reference measurement channel 12.2 kbps

Parameter	Unit	Level
Information bit rate	kbps	12.2
DPDCH	kbps	60
DPCCH	kbps	15
DPCCH Slot Format #i	–	0
DPCCH/DPDCH power ratio	dB	–2.69
TFCI	–	On
Repetition	%	23

Table 3.1.1-3 Transport channel parameters for UL reference measurement channel 12.2 kbps

Parameter	DTCH	DCCH
Transport Channel Number	1	2
Transport Block Size	244	100
Transport Block Set Size	244	100
Transmission Time Interval	20 ms	40 ms
Type of Error Protection	Convolution Coding	Convolution Coding
Coding Rate	1/3	1/3
Rate Matching attribute	256	256
Size of CRC	16	12

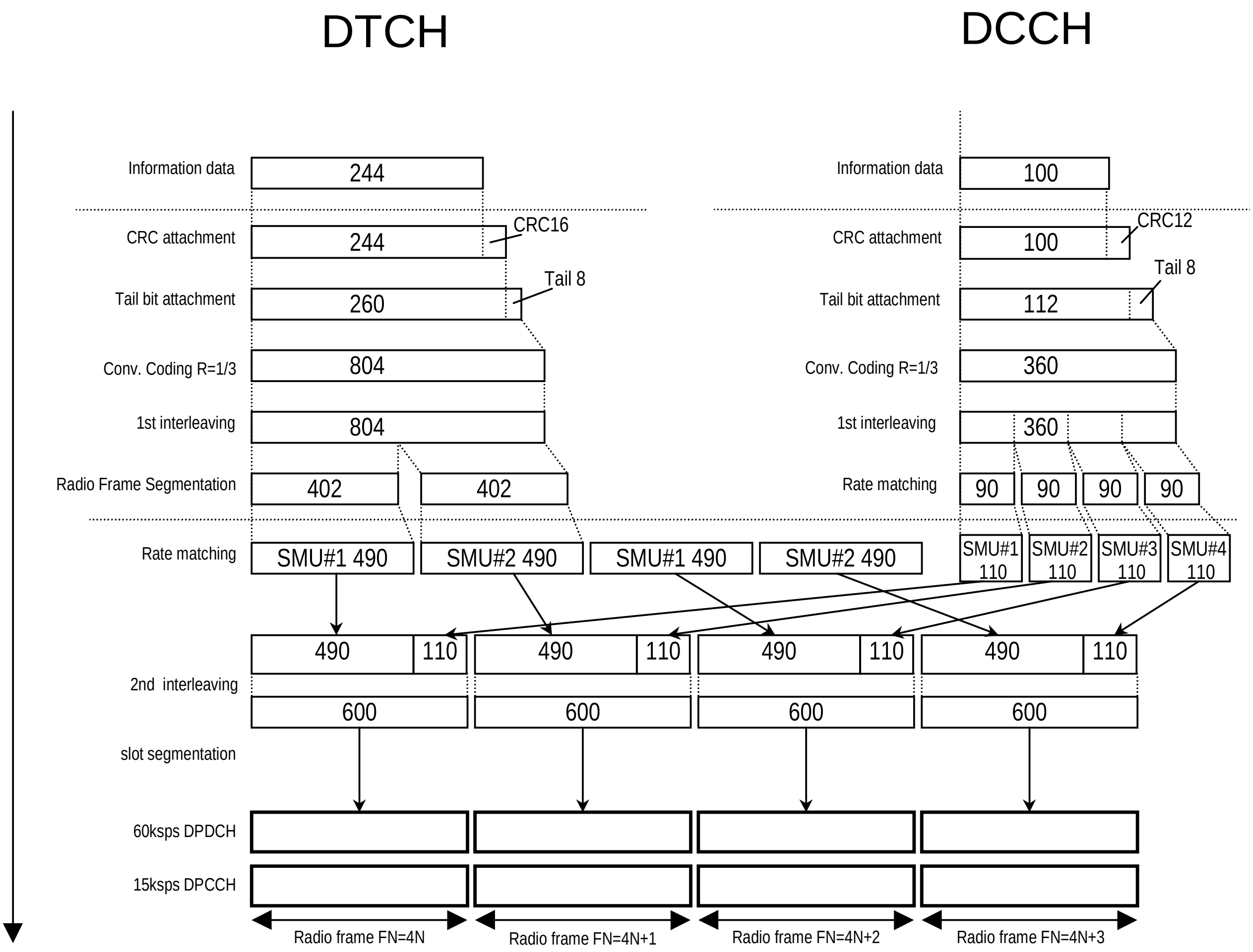


Figure 3.1.1-1 Channel coding for UL reference measurement channel (12.2 kbps)

♦ Channel coding parameters for UL_RMC_12_2kbps_TX

Table 3.1.1-4 Physical channel parameters for UL reference measurement channel 12.2 kbps for Tx test

Parameter	Unit	Level
Information bit rate	kbps	12.2
DPDCH	kbps	60
DPCCH	kbps	15
DPCCH Slot Format #i	–	0
DPCCH/DPDCH power ratio	dB	–5.46
TFCI	–	On
Repetition	%	23

Table 3.1.1-5 Transport channel parameters for UL reference measurement channel 12.2 kbps for Tx test

Parameters	DTCH	DCCH
Transport Channel Number	1	2
Transport Block Size	244	100
Transport Block Set Size	244	100
Transmission Time Interval	20 ms	40 ms
Type of Error Protection	Convolution Coding	Convolution Coding
Coding Rate	1/3	1/3
Rate Matching attribute	256	256
Size of CRC	16	12

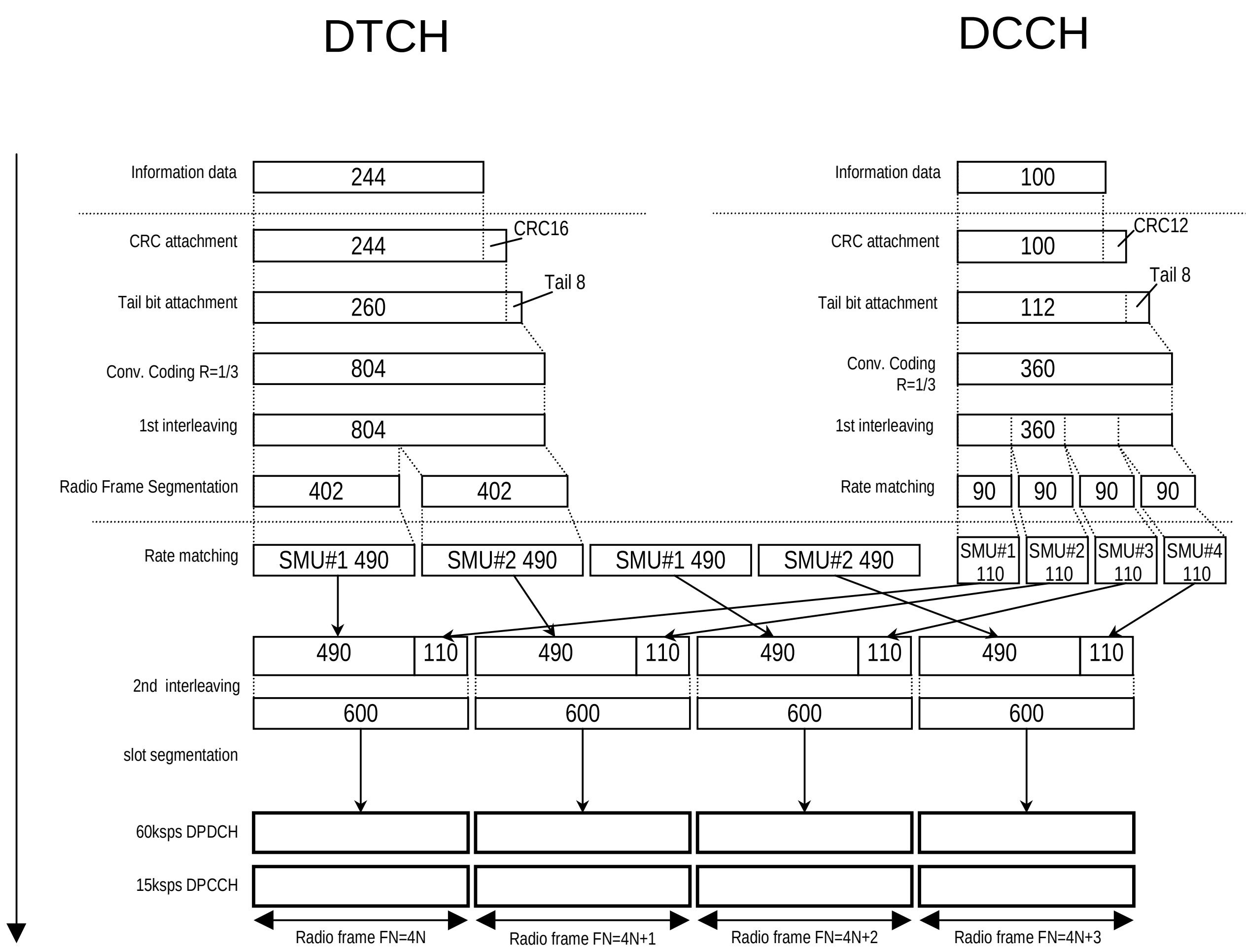


Figure 3.1.1-2 Channel coding for UL reference measurement channel (12.2 kbps)

♦ Channel coding parameters for UL_RMC_64kbps

Table 3.1.1-6 Physical channel parameters for UL reference measurement channel 64 kbps

Parameter	Unit	Level
Information bit rate	kbps	64
DPDCH	kbps	240
DPCCH	kbps	15
DPCCH Slot Format #i	–	0
DPCCH/DPDCH power ratio	dB	–5.46
TFCI	–	On
Repetition	%	18

Table 3.1.1-7 Transport channel parameters for UL reference measurement channel 64 kbps

Parameter	DTCH	DCCH
Transport Channel Number	1	2
Transport Block Size	2560	100
Transport Block Set Size	2560	100
Transmission Time Interval	40 ms	40 ms
Type of Error Protection	Turbo Coding	Convolution Coding
Coding Rate	1/3	1/3
Rate Matching attribute	256	256
Size of CRC	16	12

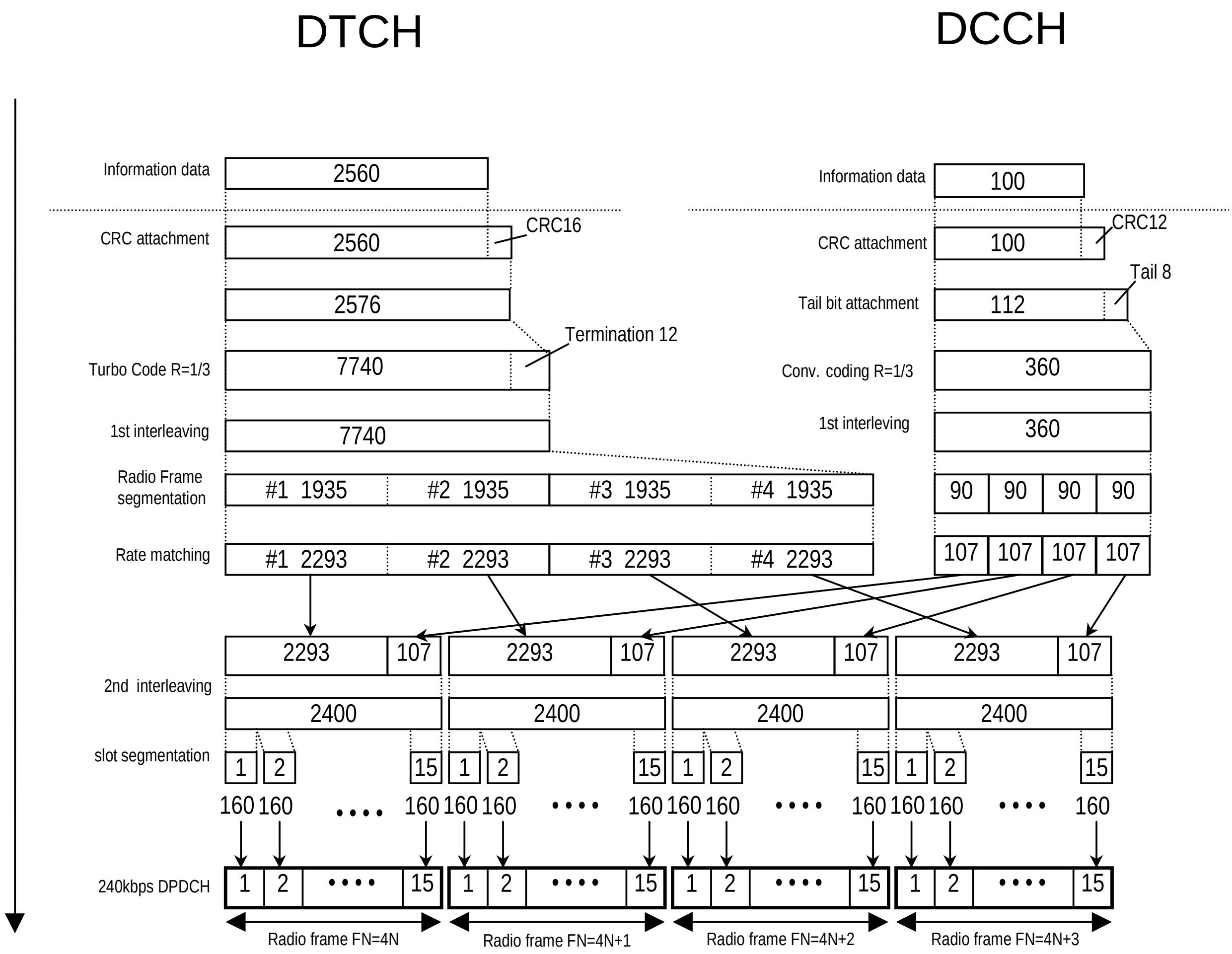


Figure 3.1.1-3 Channel coding for UL reference measurement channel (64 kbps)

♦ Channel coding parameters for UL_RMC_144kbps

Table 3.1.1-8 Physical channel parameters for UL reference measurement channel 144 kbps

Parameter	Unit	Level
Information bit rate	kbps	144
DPDCH	kbps	480
DPCCH	kbps	15
DPCCH Slot Format #i	–	0
DPCCH/DPDCH power ratio	dB	–9.54
TFCI	–	On
Repetition	%	8

Table 3.1.1-9 Transport channel parameters for UL reference measurement channel 144 kbps

Parameter	DTCH	DCCH
Transport Channel Number	1	2
Transport Block Size	2880	100
Transport Block Set Size	5760	100
Transmission Time Interval	40 ms	40 ms
Type of Error Protection	Turbo Coding	Convolution Coding
Coding Rate	1/3	1/3
Rate Matching attribute	256	256
Size of CRC	16	12

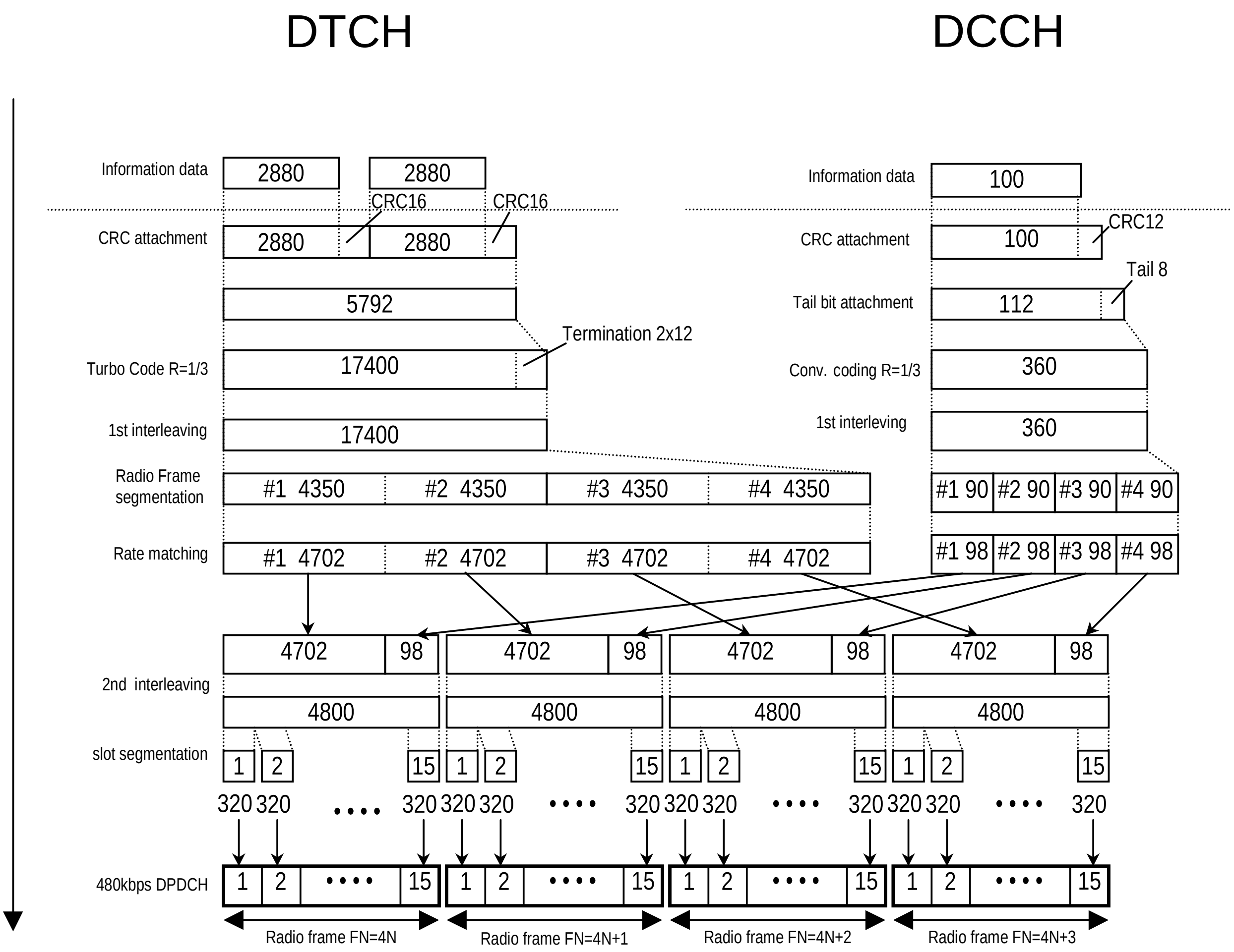


Figure 3.1.1-4 Channel coding for UL reference measurement channel (144 kbps)

♦ Channel coding parameters for UL_RMC_384kbps

Table 3.1.1-10 Physical channel parameters for UL reference measurement channel 384 kbps

Parameter	Unit	Level
Information bit rate	kbps	384
DPDCH	kbps	960
DPCCH	kbps	15
DPCCH Slot Format #i	–	0
DPCCH/DPDCH power ratio	dB	–9.54
TFCI	–	On
Puncturing	%	18

Table 3.1.1-11 Transport channel parameters for UL reference measurement channel 384 kbps

Parameter	DTCH	DCCH
Transport Channel Number	1	2
Transport Block Size	3840	100
Transport Block Set Size	15360	100
Transmission Time Interval	40 ms	40 ms
Type of Error Protection	Turbo Coding	Convolution Coding
Coding Rate	1/3	1/3
Rate Matching attribute	256	256
Size of CRC	16	12

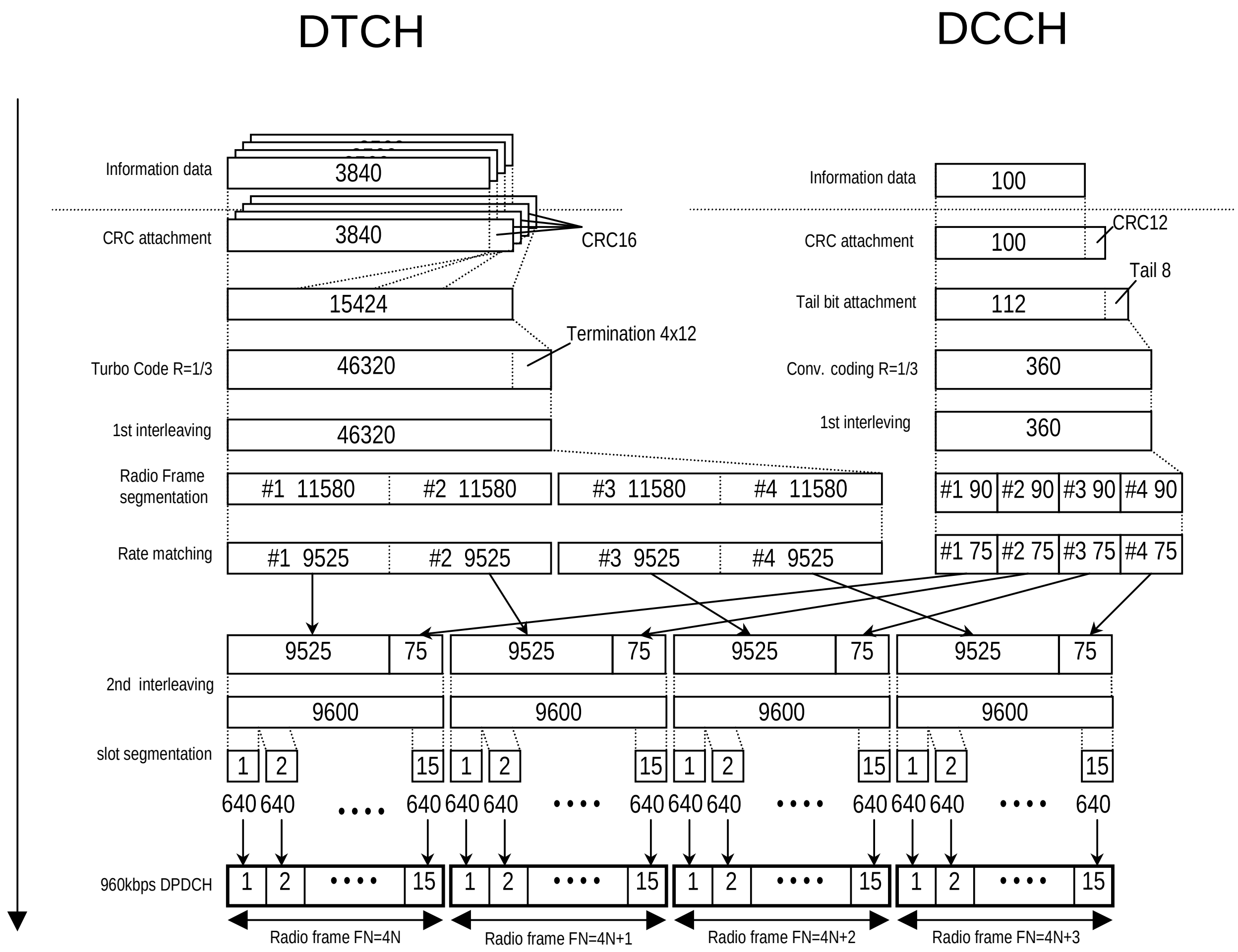


Figure 3.1.1-5 Channel coding for UL reference measurement channel (384 kbps)

3.1.2 UL_AMR_TFCSx/UL_ISDN/UL_64kbps_Packet

These waveform patterns execute channel coding, division and spreading to physical channels, and power setting conforming to the Channel coding and multiplexing example (Uplink) standard described in 3GPP TS 25.944 Section 4.1.2.

Table 3.1.2-1 lists the parameters commonly used by each waveform pattern. When outputting each waveform pattern, marker signal (Marker 1, Marker 2) as outlined in the Table 3.1.2-1 is output from Marker1 Output connector of MG3710A rear panel or from AUX connector. For details of output connector setting, refer to 7.4.2 "Route Output Connectors" in MG3710A Vector Signal Generator Operation Manual (Mainframe).

Table 3.1.2-1 List of common parameters

Parameter	Setting Value
Scrambling Code	0_H
DTCH Information Data	PN9
DCCH Information Data	All 0
Over sampling rate	3
Marker 1	Frame Clock
Marker 2	Slot Clock
Marker 3	–
AWGN addition (Note)	Enable

♦ Channel coding parameters for UL_AMR_TFCSx

Table 3.1.2-2 Physical channel parameters for UL_AMR_TFCSx

Parameter	Unit	Level
DPDCH	kbps	60
DPCCH	kbps	15
DPCCH Slot Format #i	–	0
DPCCH/DPDCH power ratio	dB	–2.69

Table 3.1.2-3 Parameters for 3.4 kbps data (DCCH)

Transport Block Size	148 bits
Transport Block Set Size	148 bits
Rate Matching attribute	160
CRC	16 bits
Coding	CC, coding rate = 1/3
TTI	40 ms

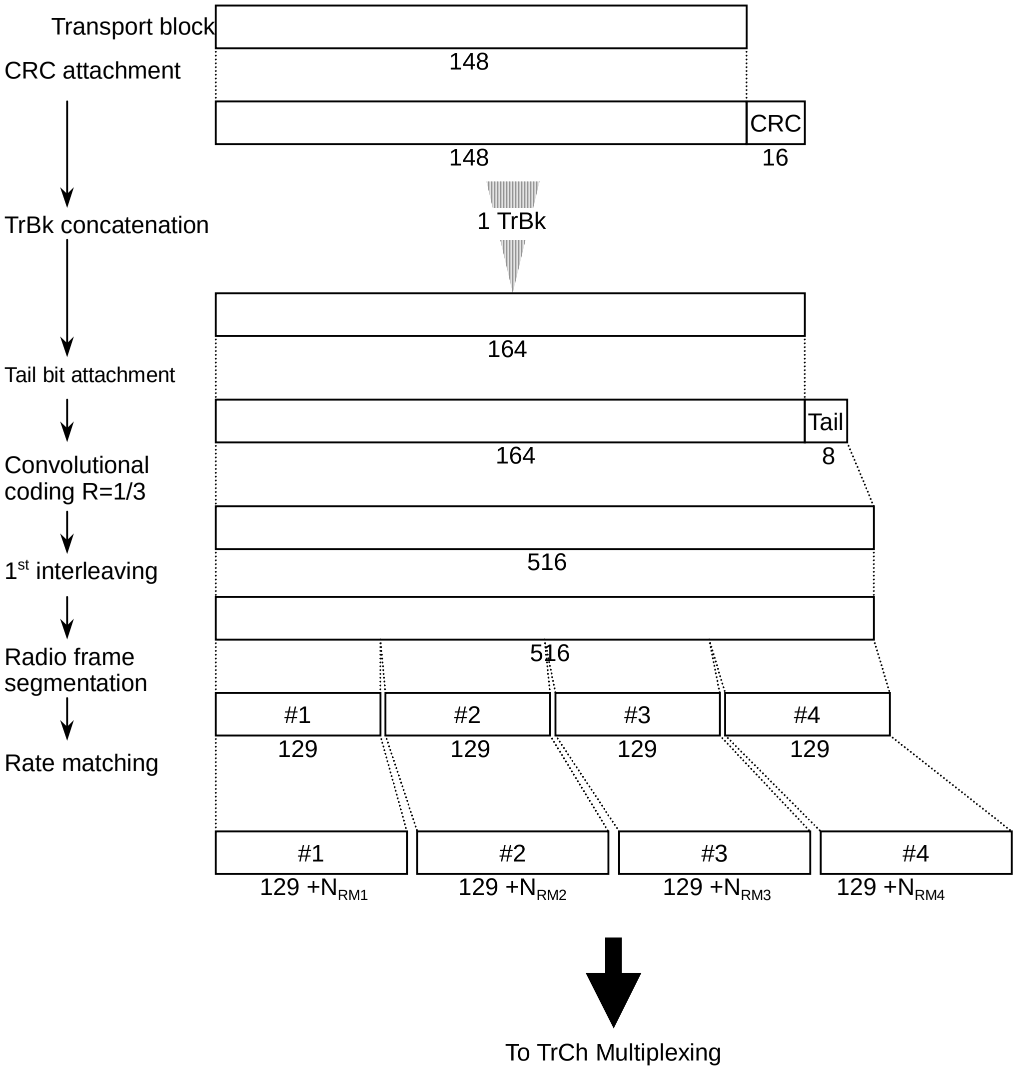
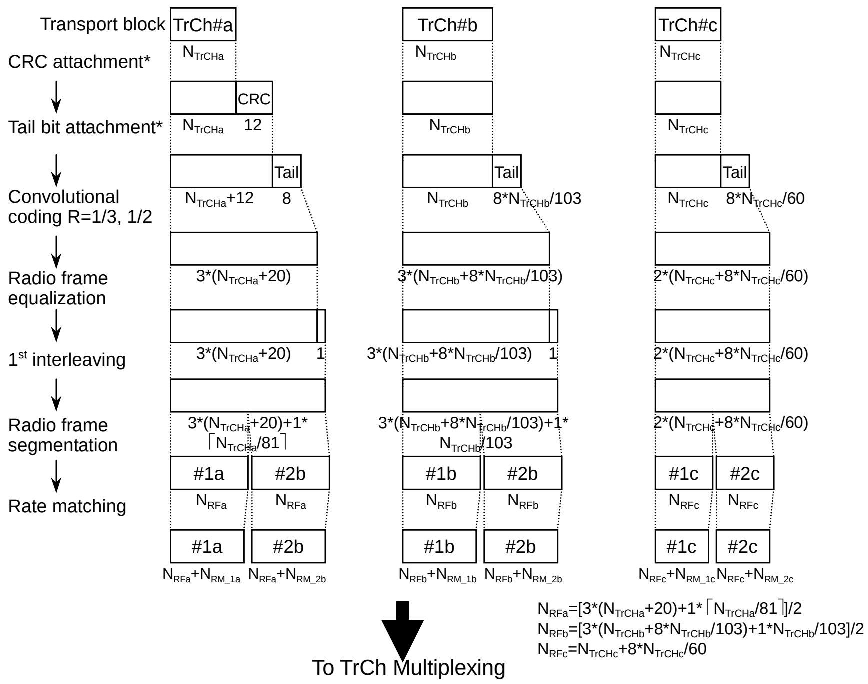


Figure 3.1.2-1 Channel coding and multiplexing for UL AMR TFCSx (1 of 2)

Table 3.1.2-4 Parameters for 12.2 kbps data (DTCH)

Number of TrCHs		3
Transport Block Size	TrCH#a	39 or 81 bits
	TrCH#b	103 bits
	TrCH#c	60 bits
TFCS	#1	N_{TrCHa} = 1*81, N_{TrCHb} = 1*103, N_{TrCHc} = 1*60 bits
	#2	N_{TrCHa} = 1*39, N_{TrCHb} = 0*103, N_{TrCHc} = 0*60 bits
	#3	N_{TrCHa} = 0*81, N_{TrCHb} = 0*103, N_{TrCHc} = 0*60 bits
Rate Matching attribute		RM_a=200, RM_b=190, RM_c=235
CRC		12 bits (attached to TrCH#a only)
Coding		CC, coding rate = 1/3 for TrCH#a, b coding rate = 1/2 for TrCH#c
TTI		20 ms



* CRC and tail bits for TrCH#a is attached even if N_{TrCha}=0 bits since CRC parity bit attachment for 0 bit transport block is applied.

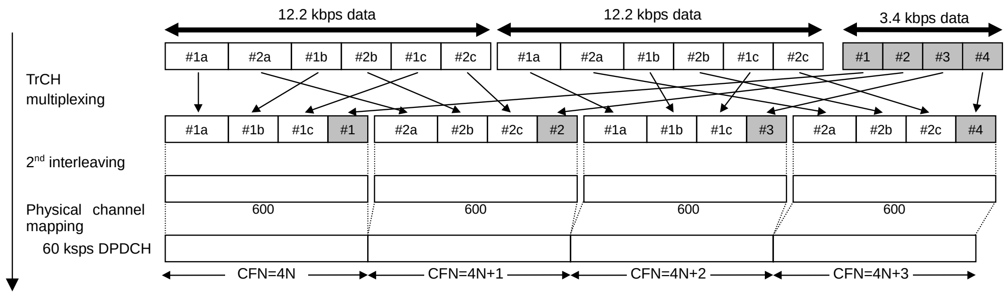


Figure 3.1.2-2 Channel coding and multiplexing for UL AMR TFCSx (2 of 2)

♦ Channel coding parameters for UL_ISDN

Table 3.1.2-5 Physical channel parameters for UL_ISDN

Parameter	Unit	Level
Information bit rate	kbps	64
DPDCH	kbps	240
DPCCH	kbps	15
DPCCH Slot Format #i	–	0
DPCCH/DPDCH power ratio	dB	–5.46

Table 3.1.2-6 Parameters for 64 kbps data

Number of TrChs	1
Transport Block Size	640 bits
Transport Block Set Size	4*640 bits
Rate Matching attribute	170
CRC	16 bits
Coding	Turbo coding, coding rate = 1/3
TTI	40 ms

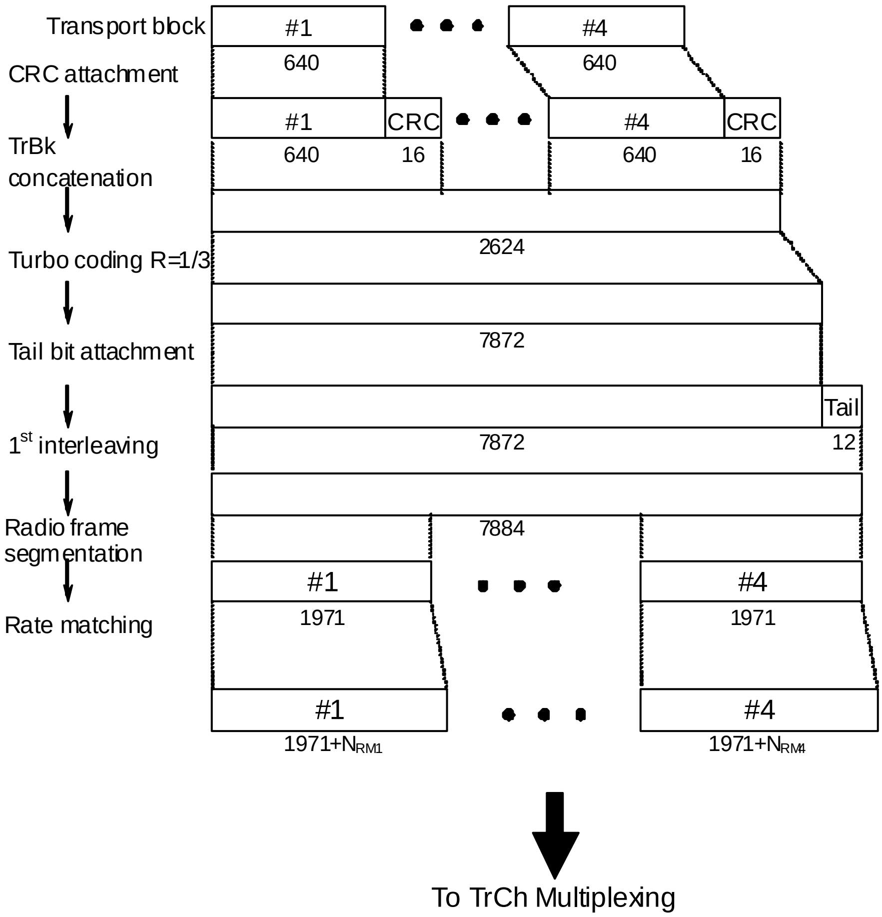


Figure 3.1.2-3 Channel coding for UL ISDN

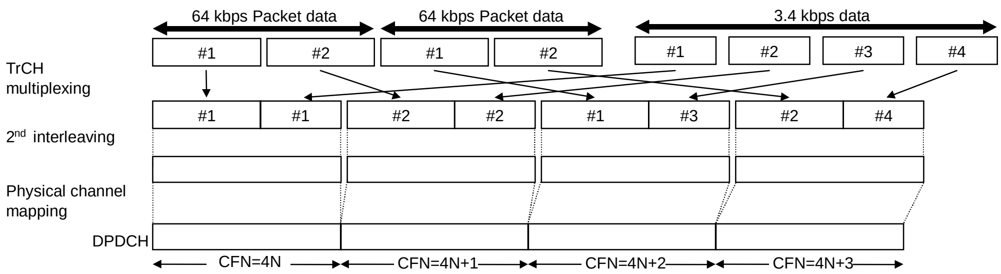


Figure 3.1.2-4 Multiplexing for UL ISDN

♦ Channel coding parameters for UL_64kbps_Packet

Table 3.1.2-7 Physical channel parameters for UL_64kbps_Packet

Parameter	Unit	Level
Information bit rate	kbps	64
DPDCH	kbps	240
DPCCH	kbps	15
DPCCH Slot Format #i	–	0
DPCCH/DPDCH power ratio	dB	–5.46

Table 3.1.2-8 Parameters for 64 kbps data

Number of TrChs		1
Transport Block Size		336 bits
Transport Block Set Size	64 kbps	336*B bits (B = 4)
Rate Matching attribute		150
CRC		16 bits
Coding		Turbo coding, coding rate = 1/3
TTI		20 ms

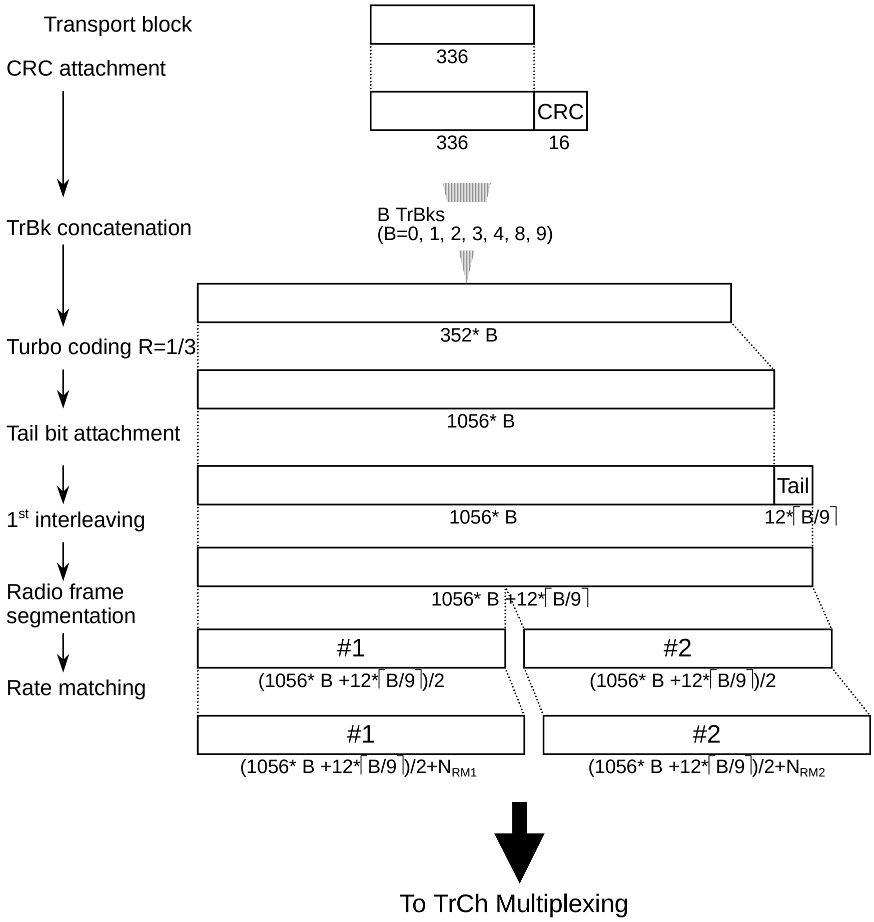


Figure 3.1.2-5 Channel coding for UL 64 kbps packet

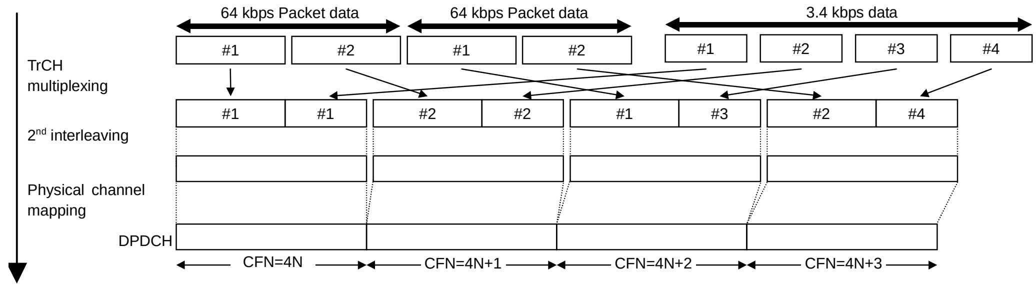


Figure 3.1.2-6 Multiplexing for UL 64 kbps packet

3.1.3 UL_Interferer

These waveform patterns execute division and spreading to physical channels, and power setting conforming to the Characteristics of the W-CDMA interference signal standard described in 3GPP TS 25.141 Annex I.

Table 3.1.3-1 UL_Interferer parameters

Parameter	Setting Value
Scrambling Code	1_H
DTCH Information Data	PN9
DCCH Information Data	All 0
Over sampling rate	4, 3 (UL_Interferer_ov3)
Marker 1	Frame Clock
Marker 2	Slot Clock
Marker 3	–

Table 3.1.3-2 Physical channel parameters for UL_Interferer

Parameter	Unit	Level
Channel Bit Rate	kbps	64
DPDCH	kbps	240
DPCCH	kbps	15
DPCCH Slot Format #i	–	0
DPCCH/DPDCH power ratio	dB	–5.46

3.1.4 DL_RMCxxxkbps

These waveform patterns execute channel coding conforming to the DL Reference Measurement Channel standard described in 3GPP TS 25.101 Annex A, and execute division and spreading to physical channels in order to generate DPCH. They also execute power setting for control channels conforming to the standard described in 3GPP TS 25.101 Annex C.

Table 3.1.4-1 lists the parameters commonly used by each waveform pattern. When outputting each waveform pattern, marker signal (Marker 1, Marker 2) as outlined in the Table 3.1.4-1 is output from Marker1 Output connector of MG3710A rear panel or from AUX connector. For details of output connector setting, refer to 7.4.2 “Route Output Connectors” in MG3710A Vector Signal Generator Operation Manual (Mainframe).

Table 3.1.4-1 List of common parameters

Parameter	Setting Value
Scrambling Code	80_H
DTCH Information Data	PN9
DCCH Information Data	All 0
SFN count	4096
Over sampling rate	4
Ch Code (P-CPICH)	0
Ch Code (P-CCPCH)	1
Ch Code (PICH)	16
Ch Code (DPCH for DL_RMC_12.2kbps)	96
Ch Code (DPCH for DL_RMC_12.2kbps_RX)	96
Ch Code (DPCH for DL_RMC_12.2kbps_MIL)	96
Ch Code (DPCH for DL_RMC_64kbps)	24
Ch Code (DPCH for DL_RMC_144kbps)	12
Ch Code (DPCH for DL_RMC_384kbps)	6
Ch Code (DPCH for DL_AMR_TFCSx)	96
Ch Code (DPCH for DL_ISDN)	24
Ch Code (DPCH for DL_384kbps_Packet)	6
OCNS	See Table 3.1.4-2.
Marker 1	TTI Pulse
Marker 2	–
Marker 3	–
AWGN addition	Enable

Table 3.1.4-2 Parameters for OCNS

Channelization Code at SF = 128	Relative Level Setting (dB)	DPCH Data
2	–1	The DPCH data for each channelization code shall be uncorrelated with each other and with any wanted signal over the period of any measurement.
11	–3	
17	–3	
23	–5	
31	–2	
38	–4	
47	–8	
55	–7	
62	–4	
69	–6	
78	–5	
85	–9	
94	–10	
125	–8	
113	–6	
119	0	

Table 3.1.4-3 Physical channel powers for DL_RMC12_2kbps_RX and DL_RMC12_2kbps_ACS

Physical Channel	Power Ratio
P-CPICH	P-CPICH_Ec/DPCH_Ec = 7 dB
P-CCPCH	P-CCPCH_Ec/DPCH_Ec = 5 dB
SCH	SCH_Ec/DPCH_Ec = 5 dB
PICH	PICH_Ec/DPCH_Ec = 2 dB
DPCH	DPCH_Ec/Ior = –10.3 dB

Table 3.1.4-4 Physical channel powers for DL_RMC12_2kbps_MIL

Physical Channel	Power ratio
P-CPICH	P-CPICH_Ec/Ior = –10 dB
P-CCPCH	P-CCPCH_Ec/Ior = –12 dB
SCH	SCH_Ec/Ior = –12 dB
PICH	PICH_Ec/Ior = –15 dB
DPCH	DPCH_Ec/Ior = –19 dB
OCNS	Power where the total power for all channels including OCNS is 0 dB

Table 3.1.4-5 Physical channel powers for DL_RMCxxxkbps (other than DL_RMC12_2kbps_RX, DL_RMC12_2kbps_ACS and DL_RMC12_2kbps_MIL)

Physical Channel		Power ratio
P-CPICH		P-CPICH_Ec/Ior = –10 dB
P-CCPCH		P-CCPCH_Ec/Ior = –12 dB
SCH		SCH_Ec/Ior = –12 dB
PICH		PICH_Ec/Ior = –15 dB
DPCH	12.2 kbps	DPCH_Ec/Ior = –16.6 dB
	64 kbps	DPCH_Ec/Ior = –12.8 dB
	144 kbps	DPCH_Ec/Ior = –9.8 dB
	384 kbps	DPCH_Ec/Ior = –5.5 dB
OCNS		Power where the total power for all channels including OCNS is 0 dB

♦ Channel coding parameters for DL_RMC_12_2kbps, DL_RMC_12_2kbps_RX, DL_RMC_12_2kbps_ACS and DL_RMC_12_2kbps_MIL

Table 3.1.4-6 Physical channel parameters for DL reference measurement channel 12.2 kbps

Parameter	Unit	Level
Information bit rate	kbps	12.2
DPCH	ksps	30
Slot Format #i	–	11
TFCI	–	On
Power offsets PO1, PO2 and PO3	dB	0
Puncturing	%	14.7

Table 3.1.4-7 Transport channel parameters for DL reference measurement channel 12.2 kbps

Parameter	DTCH	DCCH
Transport Channel Number	1	2
Transport Block Size	244	100
Transport Block Set Size	244	100
Transmission Time Interval	20 ms	40 ms
Type of Error Protection	Convolution Coding	Convolution Coding
Coding Rate	1/3	1/3
Rate Matching attribute	256	256
Size of CRC	16	12

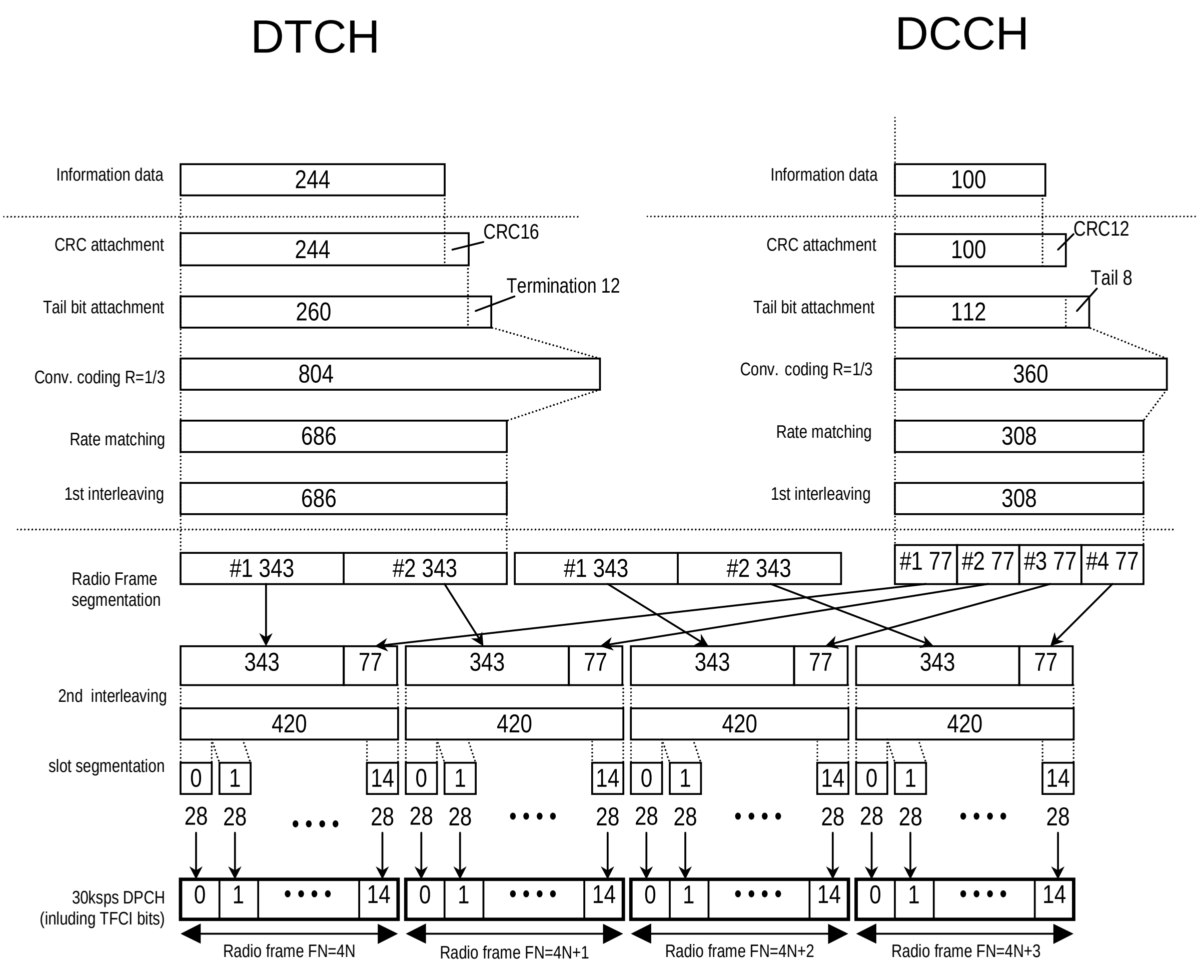


Figure 3.1.4-1 Channel coding for DL reference measurement channel (12.2 kbps)

♦ Channel coding parameters for DL_RMC_64kbps

Table 3.1.4-8 Physical channel parameters for DL reference measurement channel 64 kbps

Parameter	Unit	Level
Information bit rate	kbps	64
DPCH	ksps	120
Slot Format #i	–	13
TFCI	–	On
Power offsets PO1, PO2 and PO3	dB	0
Repetition	%	2.9

Table 3.1.4-9 Transport channel parameters for DL reference measurement channel 64 kbps

Parameter	DTCH	DCCH
Transport Channel Number	1	2
Transport Block Size	1280	100
Transport Block Set Size	1280	100
Transmission Time Interval	20 ms	40 ms
Type of Error Protection	Turbo Coding	Convolution Coding
Coding Rate	1/3	1/3
Rate Matching attribute	256	256
Size of CRC	16	12
Position of TrCH in radio frame	fixed	fixed

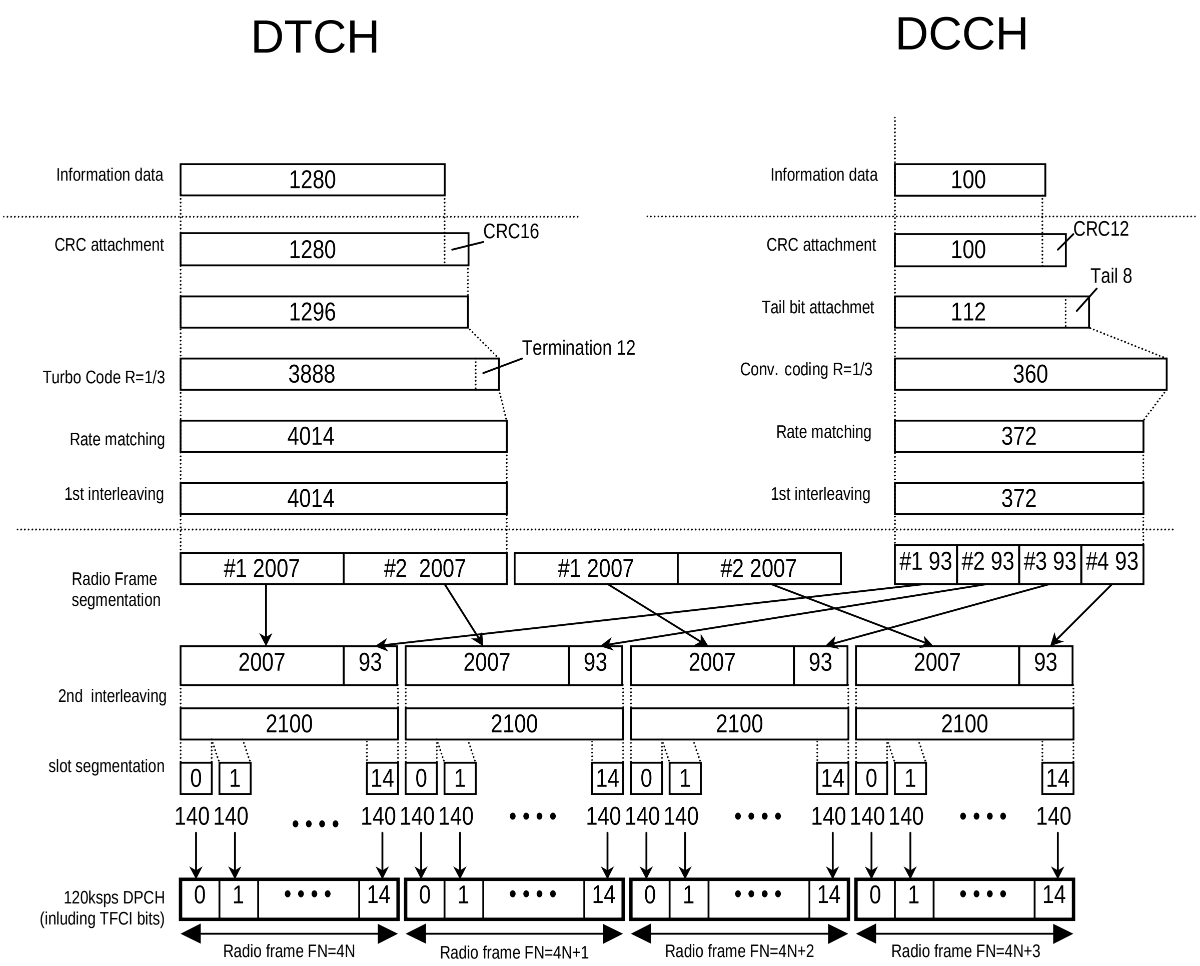


Figure 3.1.4-2 Channel coding for DL reference measurement channel (64 kbps)

♦ Channel coding parameters for DL_RMC_144kbps

Table 3.1.4-10 Physical channel parameters for DL reference measurement channel 144 kbps

Parameter	Unit	Level
Information bit rate	kbps	144
DPCH	ksps	240
Slot Format #i	–	14
TFCI	–	On
Power offsets PO1, PO2 and PO3	dB	0
Puncturing	%	2.7

Table 3.1.4-11 Transport channel parameters for DL reference measurement channel 144 kbps

Parameter	DTCH	DCCH
Transport Channel Number	1	2
Transport Block Size	2880	100
Transport Block Set Size	2880	100
Transmission Time Interval	20 ms	40 ms
Type of Error Protection	Turbo Coding	Convolution Coding
Coding Rate	1/3	1/3
Rate Matching attribute	256	256
Size of CRC	16	12
Position of TrCH in radio frame	fixed	fixed

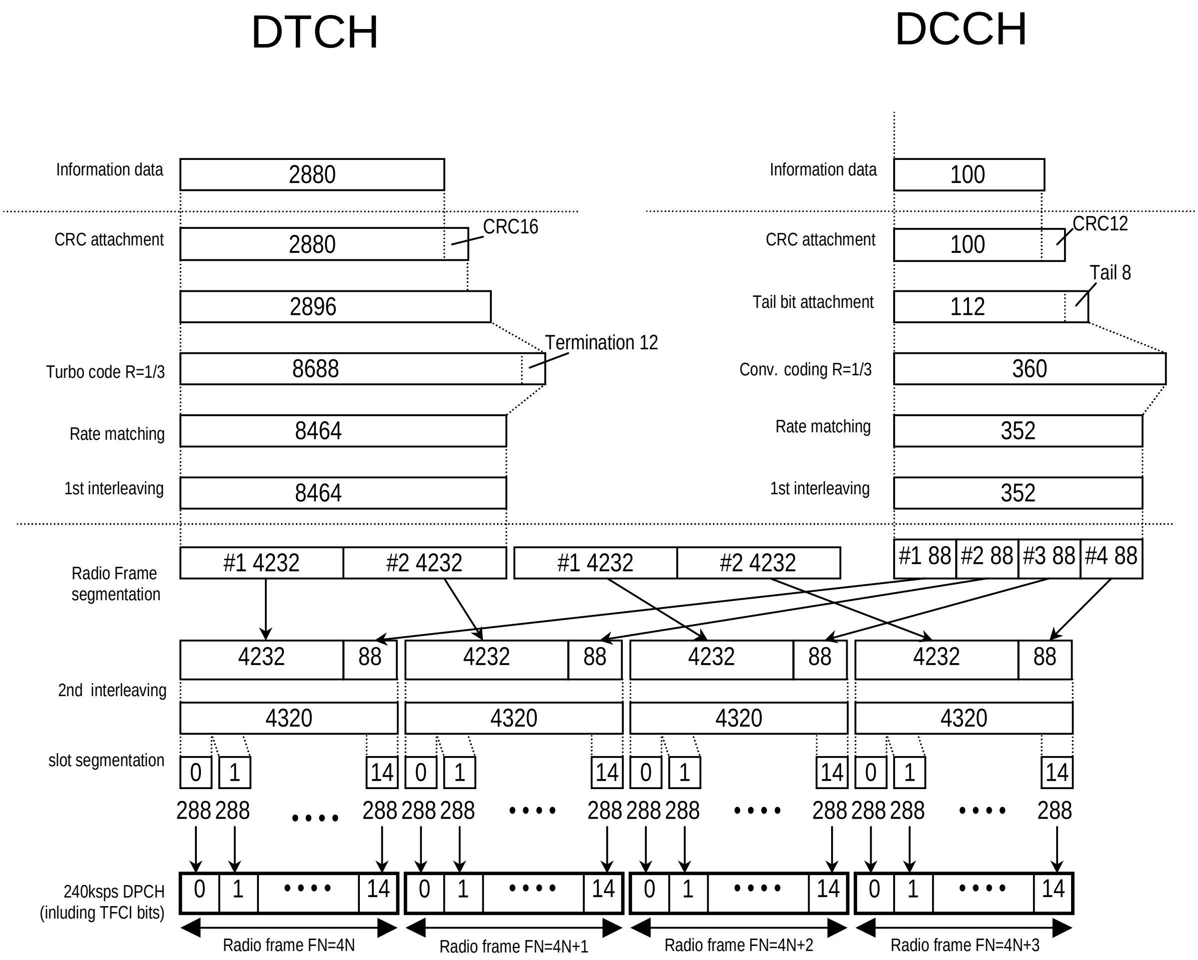


Figure 3.1.4-3 Channel coding for DL reference measurement channel (144 kbps)

♦ Channel coding parameters for DL_RMC_384kbps

Table 3.1.4-12 Physical channel parameters for DL reference measurement channel 384 kbps

Parameter	Unit	Level
Information bit rate	kbps	384
DPCH	ksps	480
Slot Format #i	–	15
TFCI	–	On
Power offsets PO1, PO2 and PO3	dB	0
Puncturing	%	22

Table 3.1.4-13 Transport channel parameters for DL reference measurement channel 384 kbps

Parameter	DTCH	DCCH
Transport Channel Number	1	2
Transport Block Size	3840	100
Transport Block Set Size	3840	100
Transmission Time Interval	10 ms	40 ms
Type of Error Protection	Turbo Coding	Convolution Coding
Coding Rate	1/3	1/3
Rate Matching attribute	256	256
Size of CRC	16	12
Position of TrCH in radio frame	fixed	fixed

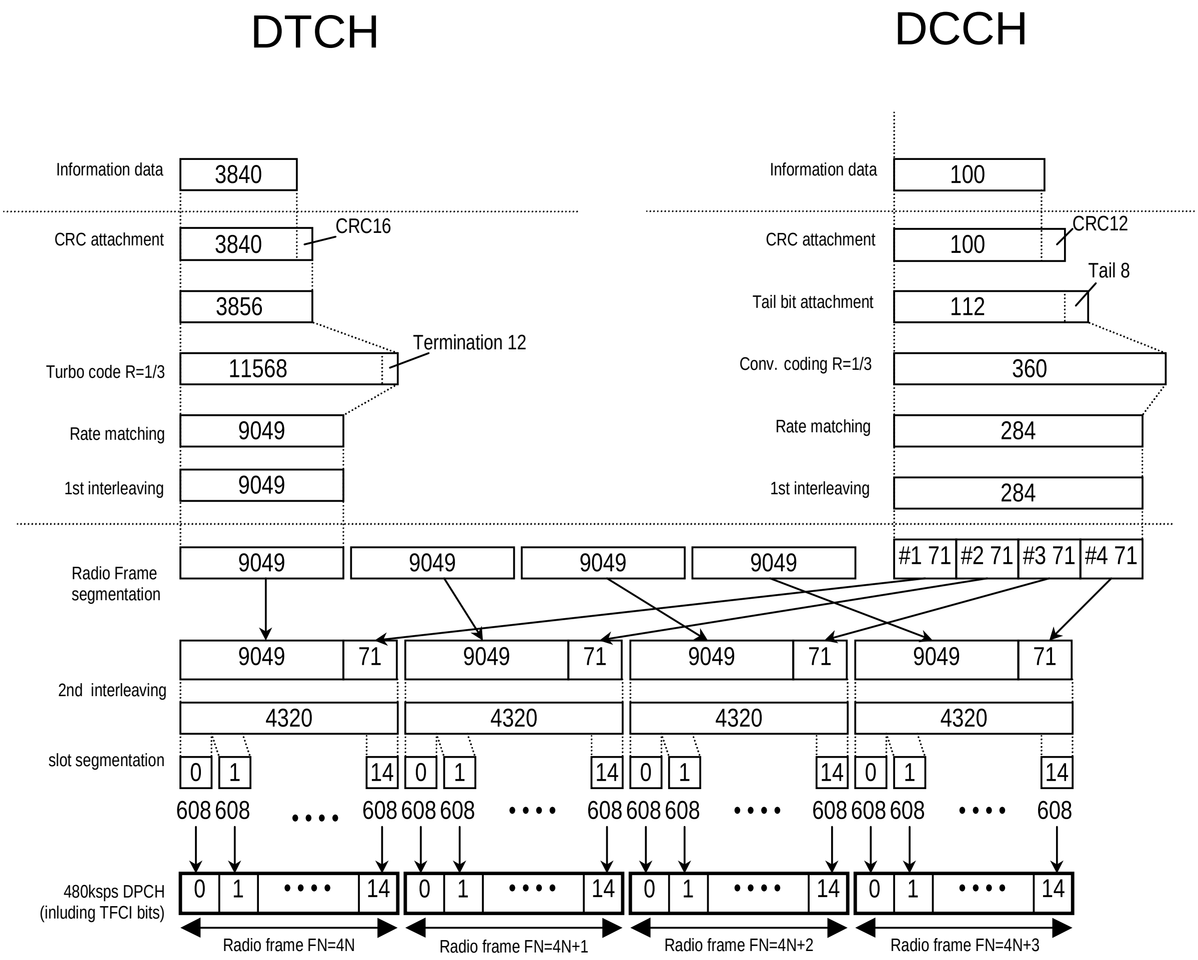


Figure 3.1.4-4 Channel coding for DL reference measurement channel (384 kbps)

3.1.5 DL_AMR_TFCSx/DL_ISDN/DL_384kbps_Packet

These waveform patterns execute channel coding, division and spreading to physical channels, and power setting conforming to the Channel coding and multiplexing example (FDD, Downlink) standard described in 3GPP TS 25.944 Section 4.1.1.

Table 3.1.5-1 lists the parameters commonly used by each waveform pattern. When outputting each waveform pattern, marker signal (Marker 1, Marker 2) as outlined in the Table 3.1.5-1 is output from Marker1 Output connector of MG3710A rear panel or from AUX connector. For details of output connector setting, refer to 7.4.2 "Route Output Connectors" in MG3710A Vector Signal Generator Operation Manual (Mainframe).

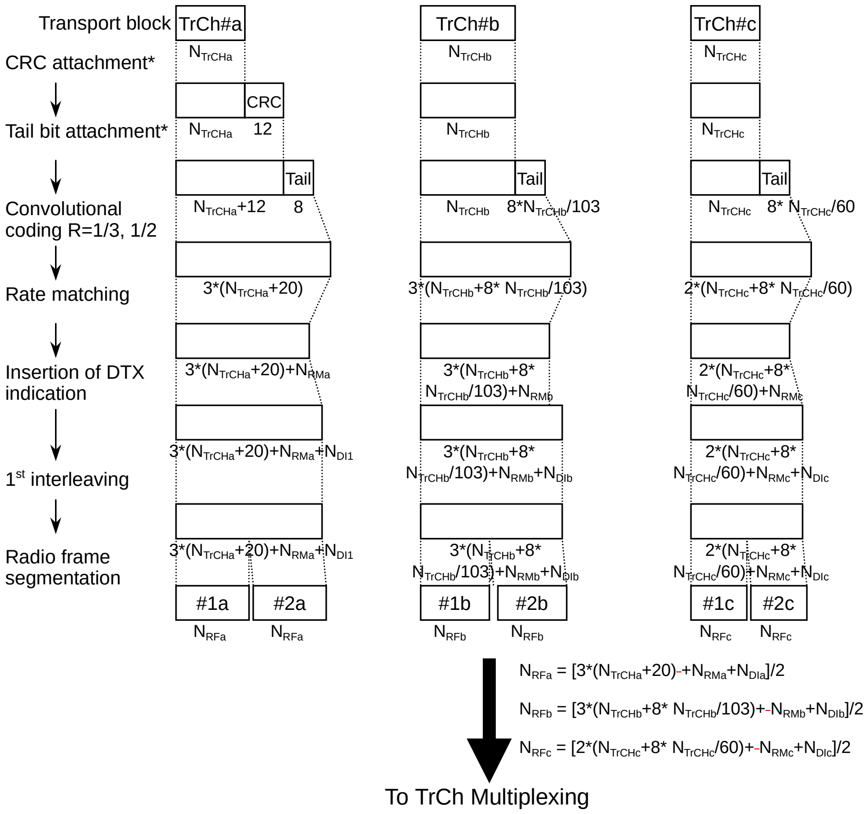
Table 3.1.5-1 List of common parameters

Parameter	Setting Value
Scrambling Code	80_H
DTCH Information Data	PN9
DCCH Information Data	All 0
Over sampling rate	4
Marker 1	TTI Clock
Marker 2	–
Marker 3	–
AWGN addition	Enable

♦ Channel coding parameters for DL_AMR_TFCSx

Table 3.1.5-2 Parameters for 12.2 kbps data

Number of TrChs		3
Transport Block Size	**TrCH#a**	0, 39 or 81 bits
	TrCH#b	103 bits
	TrCH#c	60 bits
TFCS	**#1**	N_{TrCHa} = 1*81, N_{TrCHb} = 1*103, N_{TrCHc} = 1*60 bits
	#2	N_{TrCHa} = 1*39, N_{TrCHb} = 0*103, N_{TrCHc} = 0*60 bits
	#3	N_{TrCHa} = 1*0, N_{TrCHb} = 0*103, N_{TrCHc} = 0*60 bits
Rate Matching attribute		RM_a=200, RM_b=190, RM_c=235
CRC		12 bits (attached to TrCh#a only)
CRC parity bit attachment for 0 bit transport block		Applied to TrCh#a only.
Coding		CC, coding rate = 1/3 for TrCh#a, b coding rate = 1/2 for TrCh#c
TTI		20 ms



* CRC and tail bits for TrCH#a is attached even if N_{TrCha}=0 bits since CRC parity bit attachment for 0 bit transport block is applied.

Figure 3.1.5-1 Channel coding and multiplexing for DL AMR TFCSx (1 of 2)

Table 3.1.5-3 Parameters for 3.4 kbps data

Transport Block Size	148 bits
Transport Block Set Size	148 bits
Rate Matching attribute	160
CRC	16 bits
Coding	CC, coding rate = 1/3
TTI	40 ms

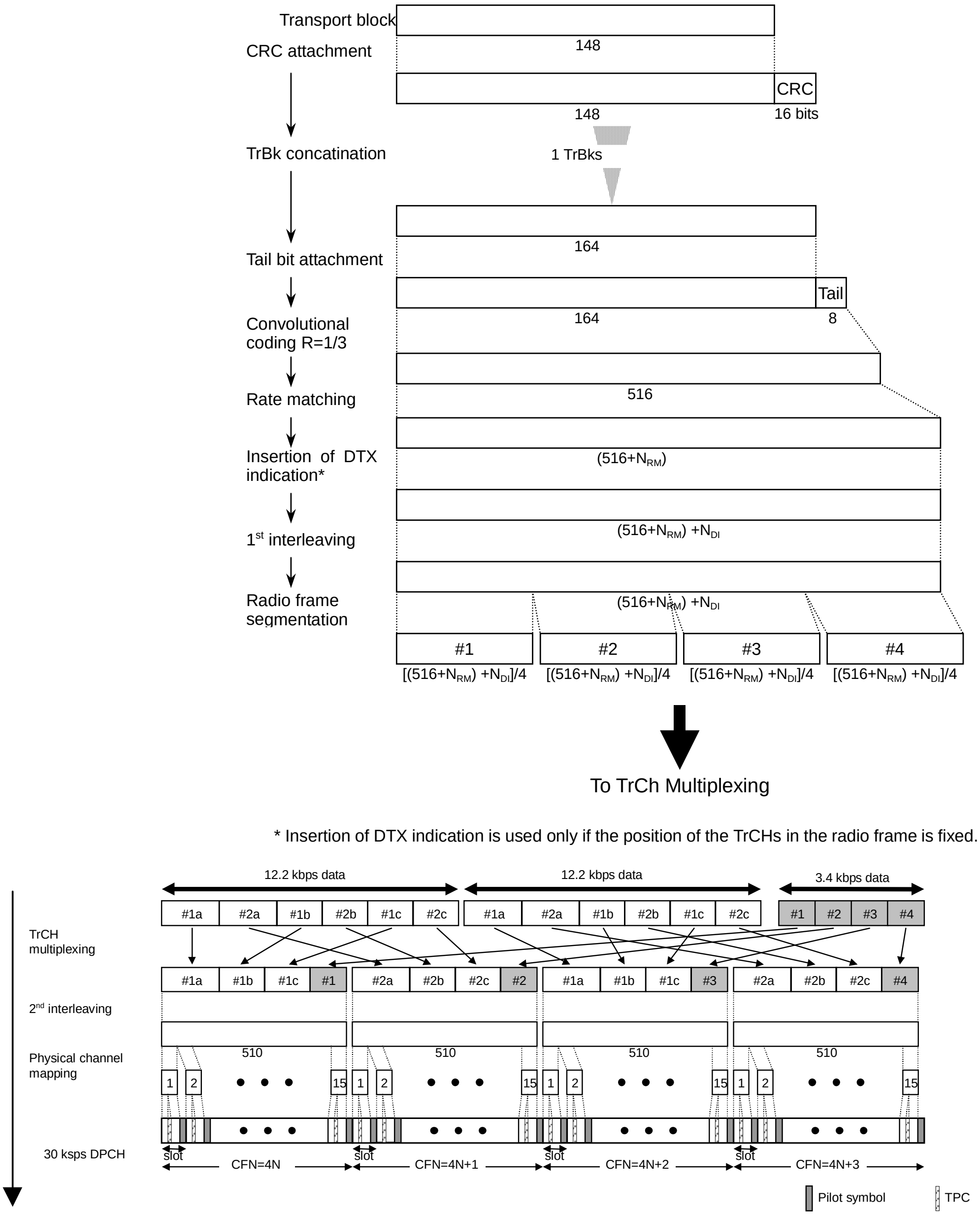


Figure 3.1.5-2 Channel coding and multiplexing for DL AMR TFCSx (2 of 2)

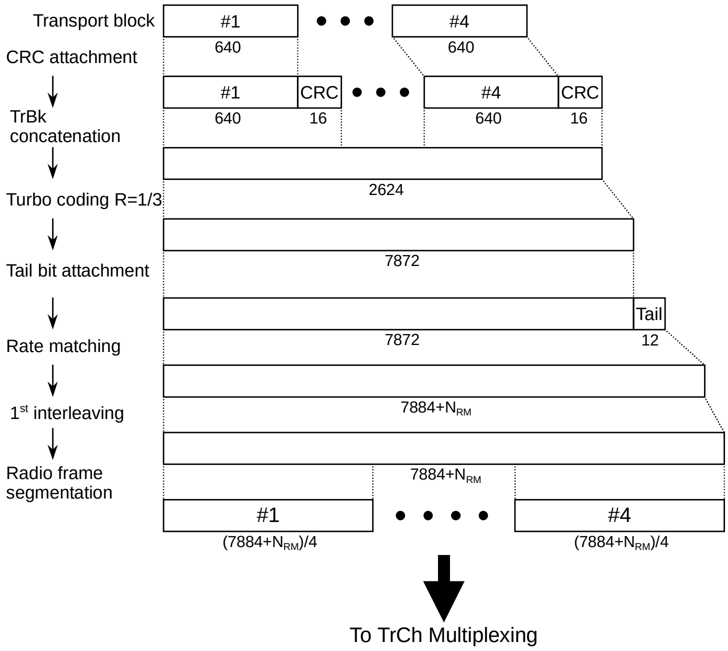
Table 3.1.5-4 Physical channel parameters for 12.2 kbps and 3.4 kbps data

Symbol Rate (ksps)	N_{pilot} (bits)	N_{TFCI} (bits)	N_{TPC} (bits)	N_{data1} (bits)	N_{data2} (bits)
30	4	0	2	6	28

♦ Channel coding parameters for DL_ISDN

Table 3.1.5-5 Parameters for 64 kbps data

Number of TrChs	1
Transport Block Size	640 bits
Transport Block Set Size	4*640 bits
Rate Matching attribute	170
CRC	16 bits
Coding	Turbo coding, coding rate = 1/3
TTI	40 ms



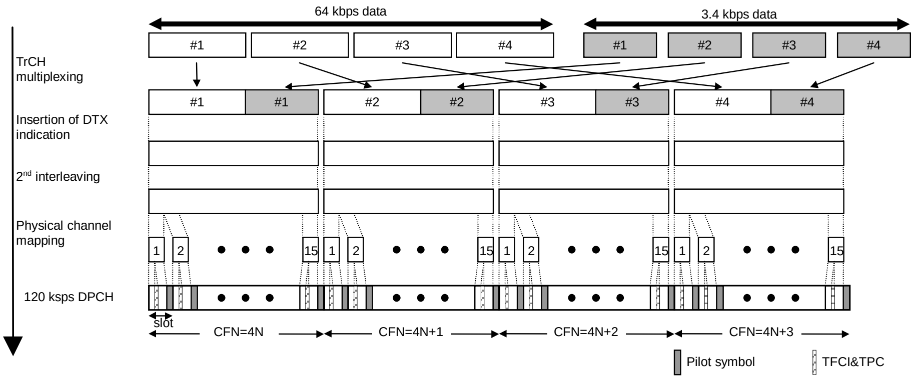


Figure 3.1.5-3 Channel coding and multiplexing for DL ISDN

Table 3.1.5-6 Physical channel parameters for 64 kbps and 3.4 kbps data

Symbol Rate (ksps)	No. of Physical Channel	N_{pilot} (bits)	N_{TFCI} (bits)	N_{TPC} (bits)	N_{data1} (bits)	N_{data2} (bits)
120	1	8	8	4	28	112

♦ Channel coding parameters for DL_384kbps_Packet

Table 3.1.5-7 Packet data parameters for 384 kbps data

Number of TrChs	1
Transport Block Size	336 bits
Transport Block Set Size	336*B bits (B = 12)
Rate Matching attribute	145
CRC	16 bits
Coding	Turbo coding, coding rate = 1/3
TTI	10 ms

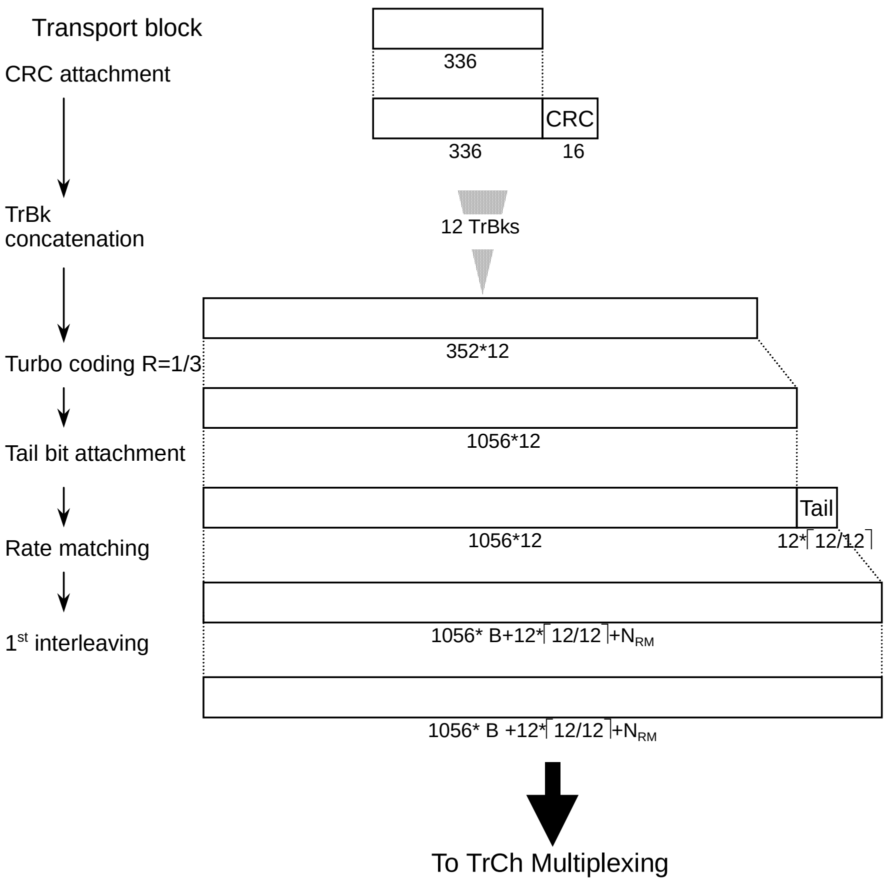


Figure 3.1.5-4 Channel coding for DL 384 kbps packet

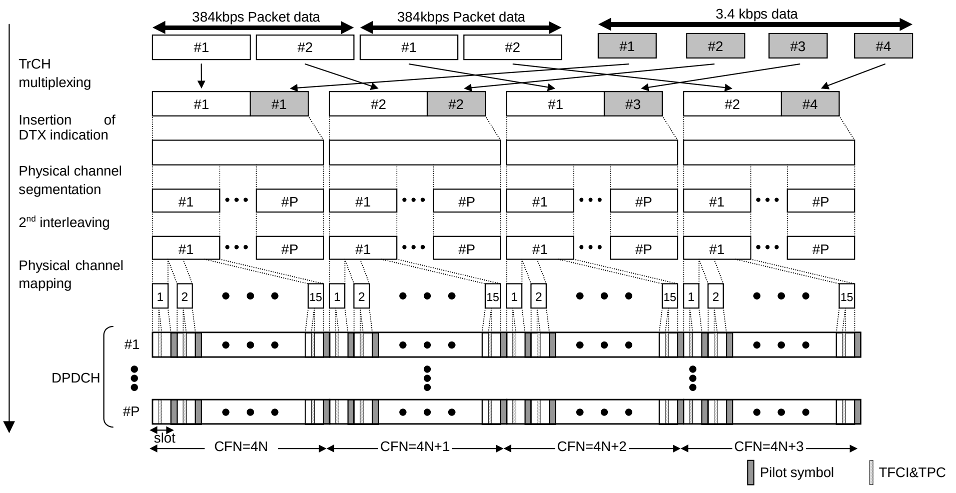


Figure 3.1.5-5 Multiplexing for DL 384 kbps

Table 3.1.5-8 Physical channel parameters for 384 kbps and 3.4 kbps data

Data Rate (kbps)	Symbol Rate (ksps)	No. of Physical Channel: P	N_{pilot} (bits)	N_{TFCI} (bits)	N_{TPC} (bits)	N_{data1} (bits)	N_{data2} (bits)
384	480	1	16	8	8	120	488

3.1.6 DL_Interferer

DL_Interferer is a modulated signal code-multiplexed according to the parameters described in 3GPP TS25.104 Annex C.4 W-CDMA Modulated Interferer.

Table 3.1.6-1 Parameters for DL_Interferer

Parameter	Setting Value
Scrambling Code	0_H
Over sampling rate	4, 3 (DL_Interferer_ov3)

Table 3.1.6-2 Physical channel parameters for DL_Interferer

Channel Type	Spreading Factor	Channelization Code	Timing Offset ($\times 256T_{chip}$)	Power	Note
P-CCPCH	256	1	0	P-CCPCH_Ec/Ior = –10 dB	
SCH	256	–	0	SCH_Ec/Ior = –10 dB	The SCH power is equally divided and distributed into 2 channels of P-SCH and S-SCH.
P-CPICH	256	0	0	P-CPICH_Ec/Ior = –10 dB	
PICH	256	16	16	PICH_Ec/Ior = –15 dB	
OCNS	See Table 3.1.6-3.				The total power of the OCNS channel and all the channels above is 0 dB.

Table 3.1.6-3 Parameters for OCNS

Channelization Code at SF = 128	Relative Level Setting (dB)	DPCH Data
2	–1	The DPCH data for each channelization code shall be uncorrelated with each other and with any wanted signal over the period of any measurement.
11	–3	
17	–3	
23	–5	
31	–2	
38	–4	
47	–8	
55	–7	
62	–4	
69	–6	
78	–5	
85	–9	
94	–10	
125	–8	
113	–6	
119	0	

3.1.7 TestModel_x_xxDPCH

TestModel_x_xxDPCH is a downlink multiplexed signal that is code-multiplexed according to the parameters described in 3GPP TS25.141 Section 11.4.0 Test Models.

Table 3.1.7-1 List of common parameters

Parameter	Setting Value
Scrambling Code *	0_H
Over sampling rate	4

*: For offset frequency (5*N[MHz]) of multicarrier when the lowest frequency carrier is 0, the Scrambling Code of each carrier is N. Time offset for each carrier frame is N/5, 2*N/5, 3*N/5, … when setting the carrier of N=0 as the reference

♦ Test Model 1

Table 3.1.7-2 Channel configuration of Test Model 1

Type	Number of Channels	Fraction of Power (%)	Level Setting (dB)	Channelization Code	Timing Offset ($x256T_{chip}$)
P-CCPCH+SCH	1	10	–10	1	0
Primary CPICH	1	10	–10	0	0
PICH	1	1.6	–18	16	120
S-CCPCH containing PCH (SF = 256)	1	1.6	–18	3	0
DPCH (SF = 128)	4/8/16/32/64	76.8 in total	See Table 3.1.7-3.		

The multicarriers (Test_Model_1_64DPCHx2/3/4) of Test Model 1 are assigned to the offset frequency as follows:

Test_Model_1_64DPCHx2 (2 carriers):	–2.5 MHz, +2.5 MHz
Test_Model_1_64x2_10M (2 carriers):	–5 MHz, +5 MHz
Test_Model_1_64x2_15M (2 carriers):	–7.5 MHz, +7.5 MHz
Test_Model_1_64DPCHx3 (3 carriers):	0 MHz, +10 MHz, +15 MHz (+5 MHz carrier is blank.)
Test_Model_1_64DPCHx4 (4 carriers):	–7.5 MHz, –2.5 MHz, +2.5 MHz, +7.5 MHz

Table 3.1.7-3 Parameters for DPCH

Code	Timing Offset (x256Tchip)	Level settings (dB) (4 codes)	Level settings (dB) (8 codes)	Level Settings (dB) (16 codes)	Level Settings (dB) (32 codes)	Level Settings (dB) (64 codes)
2	86	-5	-7	–10	–13	–16
11	134	-	-16	–12	–13	–16
17	52	-	-	–12	–14	–16
23	45	-	-	–14	–15	–17
31	143	-	-	–11	–17	–18
38	112	-7	-11	–13	–14	–20
47	59	-	-	–17	–16	–16
55	23	-	-11	–16	–18	–17
62	1	-	-	–13	–16	–16
69	88	-	-	–15	–19	–19
78	30	-9	-10	–14	–17	–22
85	18	-	-12	–18	–15	–20
94	30	-	-	–19	–17	–16
102	61	-	-	–17	–22	–17
113	128	-	-8	–15	–20	–19
119	143	-9	-12	–9	–24	–21
7	83	-	-	–	–20	–19
13	25	-	-	–	–18	–21
20	103	-	-	–	–14	–18
27	97	-	-	–	–14	–20
35	56	-	-	–	–16	–24
41	104	-	-	–	–19	–24
51	51	-	-	–	–18	–22
58	26	-	-	–	–17	–21
64	137	-	-	–	–22	–18
74	65	-	-	–	–19	–20
82	37	-	-	–	–19	–17
88	125	-	-	–	–16	–18
97	149	-	-	–	–18	–19
108	123	-	-	–	–15	–23
117	83	-	-	–	–17	–22
125	5	-	-	–	–12	–21
4	91	-	-	–	–	–17
9	7	-	-	–	–	–18
12	32	-	-	–	–	–20

Table 3.1.7-3 Parameters for DPCH (Cont'd)

Code	Timing Offset (x256Tchip)	Level settings (dB) (4 codes)	Level settings (dB) (8 codes)	Level Settings (dB) (16 codes)	Level Settings (dB) (32 codes)	Level Settings (dB) (64 codes)
14	21	-	-	–	–	–17
19	29	-	-	–	–	–19
22	59	-	-	–	–	–21
26	22	-	-	–	–	–19
28	138	-	-	–	–	–23
34	31	-	-	–	–	–22
36	17	-	-	–	–	–19
40	9	-	-	–	–	–24
44	69	-	-	–	–	–23
49	49	-	-	–	–	–22
53	20	-	-	–	–	–19
56	57	-	-	–	–	–22
61	121	-	-	–	–	–21
63	127	-	-	–	–	–18
66	114	-	-	–	–	–19
71	100	-	-	–	–	–22
76	76	-	-	–	–	–21
80	141	-	-	–	–	–19
84	82	-	-	–	–	–21
87	64	-	-	–	–	–19
91	149	-	-	–	–	–21
95	87	-	-	–	–	–20
99	98	-	-	–	–	–25
105	46	-	-	–	–	–25
110	37	-	-	–	–	–25
116	87	-	-	–	–	–24
118	149	-	-	–	–	–22
122	85	-	-	–	–	–20
126	69	-	-	–	–	–15

♦ Test Model 2

Table 3.1.7-4 Channel configuration of Test Model 2

Type	Number of Channels	Fraction of Power (%)	Level Setting (dB)	Channelization Code	Timing Offset (x256T_{chip})
P-CCPCH+SCH	1	10	–10	1	0
Primary CPICH	1	10	–10	0	0
PICH	1	5	–13	16	120
S-CCPCH containing PCH (SF = 256)	1	5	–13	3	0
DPCH (SF = 128)	3	2 x 10, 1 x 50	2 x –10, 1 x –3	24, 72, 120	1, 7, 2

♦ Test Model 3

Table 3.1.7-5 Channel configuration of Test Model 3

Type	Number of Channels	Fraction of Power (%) 4/8/16/32	Level Setting (dB) 4/8/16/32	Channelization Code	Timing Offset (x256T_{chip})
P-CCPCH+SCH	1	15,8/15,8/12,6/7,9	-8/-8/-9/-11	1	0
Primary CPICH	1	15,8/15,8/12,6/7,9	-8/-8/-9/-11	0	0
PICH	1	2.5/2.5/5/1.6	-16/-16/-13/-18	16	120
S-CCPCH containing PCH (SF = 256)	1	2.5/2.5/5/1.6	-16/-16/-13/-18	3	0
DPCH (SF = 256)	4/8/16/32	63,4/63,4/63,7/80,4 in total	See Table 3.1.7-6.		

Table 3.1.7-6 Parameters for Test Model 3

Code	T_{offset}	Level settings(dB) (4 codes)	Level settings(dB) (8 codes)	**Level Settings (dB) (16 codes)**	**Level Settings (dB) (32 codes)**
64	86	-8	-11	–14	–16
69	134	-	-	–14	–16
74	52	-	-11	–14	–16
78	45	-	-	–14	–16
83	143	-	-	–14	–16
89	112	-8	-11	–14	–16
93	59	-	-	–14	–16
96	23	-	-11	–14	–16
100	1	-	-	–14	–16
105	88	-	-	–14	–16
109	30	-8	-11	–14	–16
111	18	-	-11	–14	–16
115	30	-	-	–14	–16
118	61	-	-	–14	–16
122	128	-	-11	–14	–16
125	143	-8	-11	–14	–16
67	83	-	-	–	–16
71	25	-	-	–	–16
76	103	-	-	–	–16
81	97	-	-	–	–16
86	56	-	-	–	–16
90	104	-	-	–	–16
95	51	-	-	–	–16
98	26	-	-	–	–16
103	137	-	-	–	–16
108	65	-	-	–	–16
110	37	-	-	–	–16
112	125	-	-	–	–16
117	149	-	-	–	–16
119	123	-	-	–	–16
123	83	-	-	–	–16
126	5	-	-	–	–16

♦ Test Model 4

Table 3.1.7-7 Channel configuration of Test Model 4

Type	Number of Channels	Fraction of Power (%)	Level Setting (dB)	Channelization Code	Timing Offset
P-CCPCH+SCH when Primary CPICH is disabled	1	100	0	1	0
P-CCPCH+SCH when Primary CPICH is enabled	1	50	-3	1	0
Primary CPICH1	1	50	-3	0	0

3.1.8 TestModel_5_xDPCH

These waveforms are downlink multiplexed signals that include HS-SCCH and HS-PDSCH equivalent to Test Model 5, which is described in 3GPP TS25.141 Section 6.1.

The settings are the same as that shown in Section 3.1.9.
Refer to 3.1.9 “TestModel_5_xHSPDSCH” for details.

3.1.9 TestModel_5_xHSPDSCH

These waveforms are downlink multiplexed signals that include HS-SCCH and HS-PDSCH equivalent to Test Model 5, which is described in 3GPP TS25.141 Section 6.1.

Table 3.1.9-1 List of common parameters

Parameter	Setting Value
Scrambling Code	0_H
Over sampling rate	4

Table 3.1.9-2 Physical Channel Power

Type	Number of Channels	Level Setting (dB)	Channelization Code	Timing Offset ($x256T_{chip}$)
P-CCPCH+SCH	1	–11	1	0
Primary CPICH	1	–11	0	0
PICH	1	–19	16	120
S-CCPCH containing PCH (SF = 256)	1	–19	3	0
DPCH (SF = 128)	30/14/6/4*	See Table 3.1.9-3.		
HS-SCCH	2	See Table 3.1.9-4.		
HS-PDSCH (16QAM)	8/4/2*	See Table 3.1.9-5.		

*: DPCH is 6 channels when HS-PDSCH is 2 channels,
4 channel or 14 channels when HS-PDSCH is 4 channels, and
30 channels when HS-PDSCH is 8 channels.

Table 3.1.9-3 Setting for DPCH

Code (SF = 128)	Timing Offset (x256Tchip)	Level Settings (dB) (30 codes)	Level Settings (dB) (14 codes)	Level Settings (dB) (6 codes)	Level settings (dB)(4 codes)
15	86	–20	–17	–17	-15
23	134	–20	–19	–15	-15
68	52	–21	–19	–15	-18
76	45	–22	–20	–18	-12
82	143	–24	–18	–16	-
90	112	–21	–20	–17	-
5	59	–23	–25	–	-
11	23	–25	–23	–	-
17	1	–23	–20	–	-
27	88	–26	–22	–	-
64	30	–24	–21	–	-
72	18	–22	–22	–	-
86	30	–24	–19	–	-
94	61	–28	–20	–	-
3	128	–27	–	–	-
7	143	–26	–	–	-
13	83	–27	–	–	-
19	25	–25	–	–	-
21	103	–21	–	–	-
25	97	–21	–	–	-
31	56	–23	–	–	-
66	104	–26	–	–	-
70	51	–25	–	–	-
74	26	–24	–	–	-
78	137	–27	–	–	-
80	65	–26	–	–	-
84	37	–23	–	–	-
88	125	–25	–	–	-
89	149	–22	–	–	-
92	123	–24	–	–	-

Table 3.1.9-4 Settings for HS-SCCH

Code (SF = 128)	Timing Offset (x256Tchip)	Level Settings (dB)
9	0	–15
29	0	–21

Table 3.1.9-5 Setting for HS-PDSCH

Code (SF = 16)	Timing Offset (x256Tchip)	Level Settings (dB) (8 codes)	Level Settings (dB) (4 codes)	Level Settings (dB) (2 codes)
4	0	–11	–8	–5
5	0	–11	–8	–
6	0	–11	–	–
7	0	–11	–	–
12	0	–11	–8	–5
13	0	–11	–8	–
14	0	–11	–	–
15	0	–11	–	–

3.1.10 TestModel_6_xHSPDSCH

These waveforms are downlink multiplexed signals that include HS-SCCH and HS-PDSCH equivalent to Test Model 6, which is described in 3GPP TS25.141 Section 6.1.

Table 3.1.10-1 List of common parameters

Parameter	Setting Value
Scrambling Code	0_H
Over sampling rate	4

Table 3.1.10-2 Channel configuration of Test Model 6

Type	Number of Channels	Level Setting (dB)	Channelization Code	Timing Offset ($x256T_{chip}$)
P-CCPCH+SCH	1	–11	1	0
Primary CPICH	1	–11	0	0
PICH	1	–19	16	120
S-CCPCH containing PCH (SF = 256)	1	–19	3	0
DPCH (SF = 128)	30/4*	See Table 3.1.10-3.		
HS-SCCH	2	See Table 3.1.10-4.		
HS-PDSCH (64QAM)	8/4*	See Table 3.1.10-5.		

*: DPCH is 4 channels when HS-PDSCH is 4 channels, and 30 channels when HS-PDSCH is 8 channels.

Table 3.1.10-3 Setting for DPCH

Code (SF = 128)	Timing Offset (x256Tchip)	Level Settings (dB) (30 codes)	Level settings(dB)(4 codes)
15	86	–17	-13
23	134	–17	-15
68	52	–18	-9
76	45	–19	-12
82	143	–21	-
90	112	–18	-
5	59	–20	-
11	23	–22	-
17	1	–20	-
27	88	–23	-
64	30	–21	-
72	18	–19	-
86	30	–21	-
94	61	–25	-
3	128	–24	-
7	143	–23	-
13	83	–24	-
19	25	–22	-
21	103	–18	-
25	97	–18	-
31	56	–20	-
66	104	–23	-
70	51	–22	-
74	26	–21	-
78	137	–24	-
80	65	–23	-
84	37	–22	-
88	125	–22	-
89	149	–22	-
92	123	–21	-

Table 3.1.10-4 Settings for HS-SCCH

Code (SF = 128)	Timing Offset (x256Tchip)	Level Settings (dB)
9	0	–15
29	0	–21

Table 3.1.10-5 Setting for HS-PDSCH

Code (SF = 16)	Timing Offset (x256Tchip)	Level Settings (dB) (8 codes)	Level settings (dB) (4 codes)
4	0	–12	-9
5	0	–12	-9
6	0	–12	-
7	0	–12	-
12	0	–12	-9
13	0	–12	-9
14	0	–12	-
15	0	–12	-

3.2 LTE Waveform Pattern

LTE waveform patterns are provided as shown in Table 3.2-1.

The parameters of E-UTRA Test Models described in chapter 6 of 3GPP TS36.141 is set. For the E-TM1.1, E-TM1.2, E-TM2, E-TM3.1, E-TM3.2, and E-TM3.3 test models, Channel Bandwidth can be respectively set to 1.4 MHz, 3 MHz, 5 MHz, 10 MHz, 15 MHz, or 20 MHz. For details about the E-UTRA Test Models parameters, see chapter 6 of 3GPP TS36.141.

Table 3.2-1 LTE Waveform Pattern List

Main Use	Test Model	Band Width	File Name
Package name: LTE_FDD (BS Tx test)			
BS Tx Test	E-TM1.1	1.4 MHz	E-TM_1-1_01M4_FDD
		3 MHz	E-TM_1-1_03M_FDD
		5 MHz	E-TM_1-1_05M_FDD
		10 MHz	E-TM_1-1_10M_FDD
		15 MHz	E-TM_1-1_15M_FDD
		20 MHz	E-TM_1-1_20M_FDD
	E-TM1.2	1.4 MHz	E-TM_1-2_01M4_FDD
		3 MHz	E-TM_1-2_03M_FDD
		5 MHz	E-TM_1-2_05M_FDD
		10 MHz	E-TM_1-2_10M_FDD
		15 MHz	E-TM_1-2_15M_FDD
		20 MHz	E-TM_1-2_20M_FDD
	E-TM2	1.4 MHz	E-TM_2_01M4_FDD
		3 MHz	E-TM_2_03M_FDD
		5 MHz	E-TM_2_05M_FDD
		10 MHz	E-TM_2_10M_FDD
		15 MHz	E-TM_2_15M_FDD
		20 MHz	E-TM_2_20M_FDD
	E-TM3.1	1.4 MHz	E-TM_3-1_01M4_FDD
		3 MHz	E-TM_3-1_03M_FDD
		5 MHz	E-TM_3-1_05M_FDD
		10 MHz	E-TM_3-1_10M_FDD
		15 MHz	E-TM_3-1_15M_FDD
		20 MHz	E-TM_3-1_20M_FDD

Table 3.2-1 LTE Waveform Pattern List (Continued)

Main Use	Test Model	Band Width	File Name
BS Tx Test	E-TM3.2	1.4 MHz	E-TM_3-2_01M4_FDD
		3 MHz	E-TM_3-2_03M_FDD
		5 MHz	E-TM_3-2_05M_FDD
		10 MHz	E-TM_3-2_10M_FDD
		15 MHz	E-TM_3-2_15M_FDD
		20 MHz	E-TM_3-2_20M_FDD
	E-TM3.3	1.4 MHz	E-TM_3-3_01M4_FDD
		3 MHz	E-TM_3-3_03M_FDD
		5 MHz	E-TM_3-3_05M_FDD
		10 MHz	E-TM_3-3_10M_FDD
		15 MHz	E-TM_3-3_15M_FDD
		20 MHz	E-TM_3-3_20M_FDD

3.3 LTE TDD Waveform Pattern

LTE TDD waveform patterns are provided as shown in Table 3.3-1.

The parameters of E-UTRA Test Models described in chapter 6 of 3GPP TS36.141 is set. For the E-TM1.1, E-TM1.2, E-TM2, E-TM3.1, E-TM3.2, and E-TM3.3 test models, Channel Bandwidth can be respectively set to 1.4 MHz, 3 MHz, 5 MHz, 10 MHz, 15 MHz, or 20 MHz. For details about the E-UTRA Test Models parameters, see chapter 6 of 3GPP TS36.141.

Table 3.3-1 LTE TDD Waveform Pattern List

Main Use	Test Model	Band Width	File Name
Package name: LTE_TDD (BS Tx test)			
BS Tx Test	E-TM1.1	1.4 MHz	E-TM_1-1_01M4_TDD
		3 MHz	E-TM_1-1_03M_TDD
		5 MHz	E-TM_1-1_05M_TDD
		10 MHz	E-TM_1-1_10M_TDD
		15 MHz	E-TM_1-1_15M_TDD
		20 MHz	E-TM_1-1_20M_TDD
	E-TM1.2	1.4 MHz	E-TM_1-2_01M4_TDD
		3 MHz	E-TM_1-2_03M_TDD
		5 MHz	E-TM_1-2_05M_TDD
		10 MHz	E-TM_1-2_10M_TDD
		15 MHz	E-TM_1-2_15M_TDD
		20 MHz	E-TM_1-2_20M_TDD
	E-TM2	1.4 MHz	E-TM_2_01M4_TDD
		3 MHz	E-TM_2_03M_TDD
		5 MHz	E-TM_2_05M_TDD
		10 MHz	E-TM_2_10M_TDD
		15 MHz	E-TM_2_15M_TDD
		20 MHz	E-TM_2_20M_TDD
	E-TM3.1	1.4 MHz	E-TM_3-1_01M4_TDD
		3 MHz	E-TM_3-1_03M_TDD
		5 MHz	E-TM_3-1_05M_TDD
		10 MHz	E-TM_3-1_10M_TDD
		15 MHz	E-TM_3-1_15M_TDD
		20 MHz	E-TM_3-1_20M_TDD

Table 3.3-1 LTE TDD Waveform Pattern List (Continued)

Main Use	Test Model	Band Width	File Name
BS Tx Test	E-TM3.2	1.4 MHz	E-TM_3-2_01M4_TDD
		3 MHz	E-TM_3-2_03M_TDD
		5 MHz	E-TM_3-2_05M_TDD
		10 MHz	E-TM_3-2_10M_TDD
		15 MHz	E-TM_3-2_15M_TDD
		20 MHz	E-TM_3-2_20M_TDD
	E-TM3.3	1.4 MHz	E-TM_3-3_01M4_TDD
		3 MHz	E-TM_3-3_03M_TDD
		5 MHz	E-TM_3-3_05M_TDD
		10 MHz	E-TM_3-3_10M_TDD
		15 MHz	E-TM_3-3_15M_TDD
		20 MHz	E-TM_3-3_20M_TDD

3.4 PDC Waveform Pattern

As the PDC waveform pattern, waveform patterns that output uplink/downlink slot 0 only at the full rate or half rate, and unframed waveform patterns for interference signals are provided as shown in Table 3.4-1.

Table 3.4-1 List of PDC waveform patterns

Waveform Pattern Name	Uplink/Downlink	Half Rate/Full Rate	Output Slot
Package name: PDC			
PI_4_DQPSK_PN9	–	–	Unframed
PI_4_DQPSK_PN15	–	–	Unframed
DL_Full_Rate_Slot0	Downlink	Full rate	Slot 0 only
DL_Half_Rate_Slot0	Downlink	Half rate	Slot 0 only
UL_Full_Rate_Slot0	Uplink	Full rate	Slot 0 only
UL_Half_Rate_Slot0	Uplink	Half rate	Slot 0 only
CW	–	–	–

When outputting each PDC waveform pattern, marker signal (Marker 1, Marker 2, Marker 3) as outlined in the Table 3.4-2 is output from Marker1 Output connector of MG3710A rear panel or from AUX connector. For details of output connector setting, refer to 7.4.2 “Route Output Connectors” in MG3710A Vector Signal Generator Operation Manual (Mainframe).

Table 3.4-2 Marker output data and IQ output level

Marker Signal	Output Data
Marker 1	Frame Clock
Marker 2	RF Gate
Marker 3	Symbol Clock

Transfer and selection of an additional waveform pattern that is generated by adding two signals, such as a desired signal + an interference signal, and using two memories, can be operated easily by selecting a combination file listed in Table 3.4-3 below when the MG3710A is in the Defined mode.

Table 3.4-3 List of combination files for PDC reception evaluation

Combination File Name	Comment
Package name: PDC_CMB	
PDC_BS_FULL_RATE_ACS	For base station adjacent channel selectivity test UL_Full_Rate_Slot0+PI_4_DQPSK_PN15 (50 kHz offset)
PDC_BS_FULL_RATE_IMD	For base station intermodulation characteristics test UL_Full_Rate_Slot0+CW (200 kHz offset) *
PDC_BS_FULL_RATE_SR	For base station spurious sensitivity test UL_Full_Rate_Slot0+CW (100 kHz offset)
PDC_BS_HALF_RATE_ACS	For base station adjacent channel selectivity test UL_Half_Rate_Slot0+PI_4_DQPSK_PN15 (50 kHz offset)
PDC_BS_HALF_RATE_IMD	For base station intermodulation characteristics test UL_Half_Rate_Slot0+CW (200 kHz offset) *
PDC_BS_HALF_RATE_SR	For base station spurious sensitivity test UL_Half_Rate_Slot0+CW (100 kHz offset)
PDC_UE_FULL_RATE_ACS	For mobile station adjacent channel selectivity test DL_Full_Rate_Slot0+PI_4_DQPSK_PN15 (50 kHz offset)
PDC_UE_FULL_RATE_IMD	For mobile station intermodulation characteristics test DL_Full_Rate_Slot0+CW (200 kHz offset) *
PDC_UE_FULL_RATE_SR	For mobile station spurious sensitivity test DL_Full_Rate_Slot0+CW (100 kHz offset)
PDC_UE_HALF_RATE_ACS	For mobile station adjacent channel selectivity test DL_Half_Rate_Slot0+PI_4_DQPSK_PN15 (50 kHz offset)
PDC_UE_HALF_RATE_IMD	For mobile station intermodulation characteristics test DL_Half_Rate_Slot0+CW (200 kHz offset) *
PDC_UE_HALF_RATE_SR	For mobile station spurious sensitivity test DL_Half_Rate_Slot0+CW (100 kHz offset)

*: The high-frequency signal generator 1 (modulated desired signal) and the high-frequency signal generator 3 (CW interference signal) are used in combination. When executing an intermodulation characteristics test, it must be externally added with a CW signal (high-frequency signal generator 2) with 100 kHz offset that is generated by another CW signal generator.

Note *:*

To use this combination file, Combination of Baseband Signal (option) is required.

3.4.1 Frame configuration

At full rate

The PDC system consists of TDMA frames that are composed of three slots, and data is generated cyclically based on one TDMA frame. A PN9 pseudo random pattern in each slot is independent within the slot and has continuity. In downlink, all 1 data are output for the bit sequence in Slots 1 and 2. In uplink, Slots 1 and 2 are burst off.

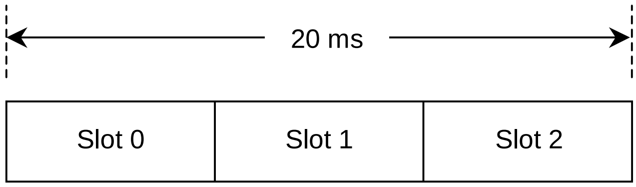


Figure 3.4.1-1 Frame configuration at full rate

At half rate

The PDC system consists of TDMA frames that are composed of six slots, and data is generated cyclically based on one TDMA frame. A PN9 pseudo random pattern in each slot is independent within the slot and has continuity. In downlink, all 1 data are output for the bit sequence in Slots 1 through 5. In uplink, Slots 1 through 5 are burst off.

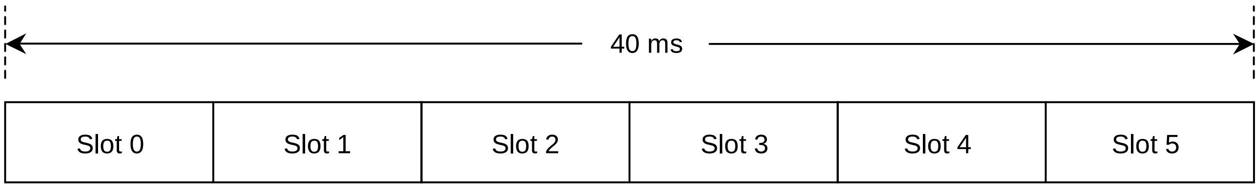


Figure 3.4.1-2 Frame configuration at half rate

Unframed waveform pattern

For interference signals, unframed pseudo random patterns are output for which $\pi/4$ DQPSK modulation was performed. At this time, the positions of the first and last symbol points of the arbitrary waveform pattern are changed to adjust the data length, so as to retain the continuity of the pseudo random pattern.

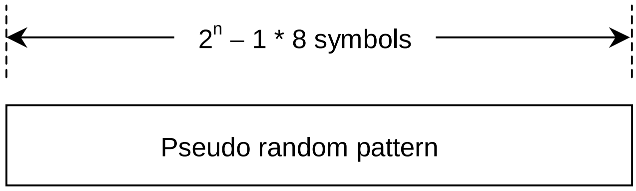


Figure 3.4.1-3 Unframed waveform pattern configuration

3.4.2 Slot configuration

There are four types of slot configurations according to the communication channels (uplink/downlink).

Uplink communication channel (UP TCH)

R	P	TCH	SW	CC	SF	SACCH	TCH	G
4	2	112	20	8	1	15	112	6

R: Guard time for burst transient response 0_H (4 bits)
P: Preamble 2_H (2 bits)
TCH: For user information transfer PN pseudo random pattern independent in each slot (PN pattern is continuous in TCH of a slot).
SW: Sync word Slot 0 = $785B4_H$ (20 bits)
Slot 1 = $62DC9_H$ (20 bits)
Slot 2 = $7E28A_H$ (20 bits)
CC: Color code 00_H (8 bits)
SF: Steal flag 0_H (1 bit)
SACCH: Low-speed associated control channel 0000H (15 bits)
G: Guard time for burst transient response 0_H (6 bits)
Scramble function (TCH, SF, SACCH): Off

Downlink communication channel (DOWN TCH)

R	P	TCH	SW	CC	SF	SACCH	TCH
4	2	112	20	8	1	21	112

R: Guard time for burst transient response 0_H (4 bits)
P: Preamble 2_H (2 bits)
TCH: For user information transfer PN pseudo random pattern independent in each slot (PN pattern is continuous in TCH of a slot).
SW: Sync word Slot 0 = $87A4B_H$ (20 bits)
Slot 1 = $9D236_H$ (20 bits)
Slot 2 = $81D75_H$ (20 bits)
CC: Color code 00_H (8 bits)
SF: Steal flag 0_H (1 bit)
SACCH: Low-speed associated control channel 000000H (21 bits)
Scramble function (TCH, SF, SACCH): Off

3.5 PDC PACKET Waveform Pattern

As the PDC PACKET waveform pattern, waveform patterns for uplink and downlink are provided as shown in Table 3.5-1.

Table 3.5-1 List of PDC PACKET waveform patterns

Waveform Pattern Name	Uplink/Downlink	Output Slot
Package name: PDC		
DL_Packet_Slot_0	Downlink	Slot 0 only
DL_Packet_Slot_01	Downlink	Slots 0 and 1
DL_Packet_Slot_all	Downlink	Slots 0, 1, and 2
UL_Packet_Slot_0	Uplink	Slot 0 only

When outputting each PDC PACKET waveform pattern, marker signal (Marker 1, Marker 2, Marker 3) as outlined in the Table 3.5-2 is output from Marker1 Output connector of MG3710A rear panel or from AUX connector. For details of output connector setting, refer to 7.4.2 “Route Output Connectors” in MG3710A Vector Signal Generator Operation Manual (Mainframe).

Table 3.5-2 Marker output data and IQ output level

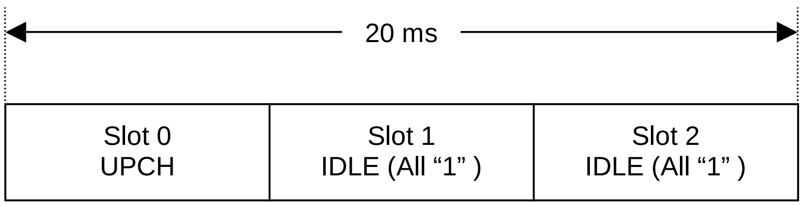
Marker Signal	Output Data
Marker 1	Frame Clock
Marker 2	RF Gate
Marker 3	Symbol Clock

3.5.1 Frame configuration

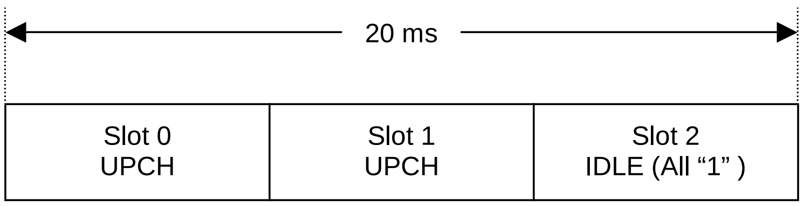
There are four types of TDMA frame configurations for PDC PACKET waveform patterns: downlink 1-slot transmission, downlink 2-slot transmission, downlink 3-slot transmission, and uplink 1-slot transmission. Each TDMA frame is composed of three slots, and data is generated cyclically based on one TDMA frame.

A PN9 pseudo random pattern in the CAC field of each slot has continuity. In downlink UPCH 2-slot transmission, for example, the end of the CAC field in Slot 0 and the start of the CAC field in Slot 1 are continuing. Also, the end of the CAC field in Slot 1 and the start of the CAC field in Slot 0 of the next frame are continuing in this case.

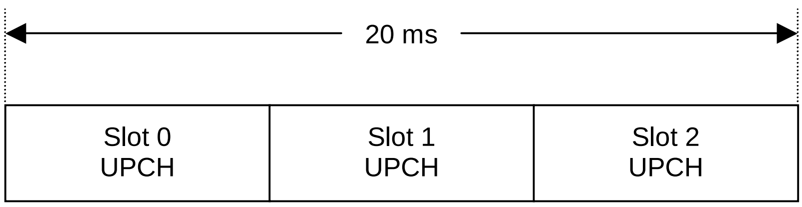
Downlink UPCH 1-slot transmission (DL_Packet_Slot_0)



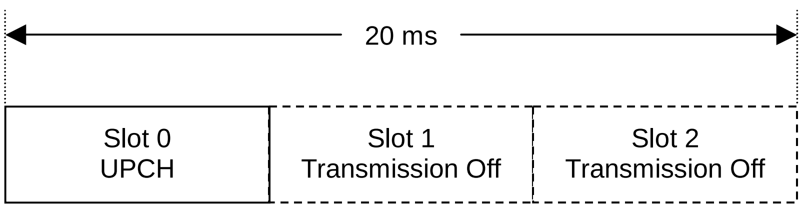
Downlink UPCH 2-slot transmission (DL_Packet_Slot_01)



Downlink UPCH 3-slot transmission (DL_Packet_Slot_all)



Uplink UPCH 1-slot transmission (UL_Packet_Slot_0)



3.5.2 Slot configuration

There are two types of slot configurations: downlink user packet channel and uplink user packet channel. The scramble function is always Off.

Downlink user packet channel (DOWN UPCH)

R 4	P 2	CAC 112	SW 20	CC 8	CAC 112	E 22

R:	Guard time for burst transient response	0_H (4 bits)
P:	Preamble	2_H (2 bits)
CAC:	Control signals (UPCH)	PN9 pseudo random pattern (continuous between transmitted slots)
SW:	Sync word	Slot 0 = $87A4B_H$ (20 bits) Slot 1 = $9D236_H$ (20 bits) Slot 2 = $81D75_H$ (20 bits)
CC:	Color code	00_H (8 bits)
E:	Collision control bits	$3FFFFF_H$ (22 bits)

Uplink user packet channel (UP UPCH)

R 4	P 2	CAC 112	SW 20	CC 8	CAC 116	G 18

R:	Guard time for burst transient response	0_H (4 bits)
P:	Preamble	2_H (2 bits)
CAC:	Control signals (UPCH)	PN9 pseudo random pattern (continuous between transmitted slots)
SW:	Sync word	Slot 0 = $785B4_H$ (20 bits)
CC:	Color code	00_H (8 bits)
G:	Guard time	00000_H (18 bits)

3.6 PHS Waveform Pattern

As the PHS waveform pattern, continuous waveform patterns for uplink/downlink TCH and interference signals are provided as shown in Table 3.6-1.

Table 3.6-1 List of PHS waveform patterns

Waveform Pattern Name	Uplink/Downlink	Scramble	Output Slot
Package name: PHS			
PI_4_DQPSK_PN9	–	OFF	Unframed
PI_4_DQPSK_PN15	–	OFF	Unframed
PI_4_DQPSK_ALL0	–	OFF	Unframed
DL_TCH_Slot_1	Downlink	OFF	Slot 1 only
UL_TCH_Slot_1	Uplink	OFF	Slot 1 only
CW	–	–	–

When outputting each PHS waveform pattern, marker signal (Marker 1, Marker 2, Marker 3) as outlined in the Table 3.6-2 is output from Marker1 Output connector of MG3710A rear panel or from AUX connector. For details of output connector setting, refer to 7.4.2 “Route Output Connectors” in MG3710A Vector Signal Generator Operation Manual (Mainframe).

Table 3.6-2 Marker output data and IQ output level

Marker Signal	Output Data
Marker 1	Frame Clock
Marker 2	RF Gate
Marker 3	Symbol Clock

Transfer and selection of an additional waveform pattern that is generated by adding two signals, such as a desired signal + an interference signal, and using two memories, can be operated easily by selecting a combination file listed in Table 3.6-3 below when the MG3710A is in the Defined mode.

Table 3.6-3 List of combination files for PHS reception evaluation

Combination File Name	Comment
Package name: PHS_CMB	
PHS_BS_ACS_0_6MHz	For base station adjacent channel selectivity test UL_TCH_Slot_1+PI_4_DQPSK_PN15 (600 kHz offset)
PHS_BS_ACS_0_9MHz	For base station adjacent channel selectivity test UL_TCH_Slot_1+PI_4_DQPSK_PN15 (900 kHz offset)
PHS_BS_IMD	For base station intermodulation characteristics test UL_TCH_Slot_1+CW (1.2 MHz offset) *
PHS_UE_ACS_0_6MHz	For mobile station adjacent channel selectivity test DL_TCH_Slot_1+PI_4_DQPSK_PN15 (600 kHz offset)
PHS_UE_ACS_0_9MHz	For mobile station adjacent channel selectivity test DL_TCH_Slot_1+PI_4_DQPSK_PN15 (900 kHz offset)
PHS_UE_IMD	For mobile station intermodulation characteristics test DL_TCH_Slot_1+CW (1.2 MHz offset) *

*: The high-frequency signal generator 1 (modulated desired signal) and the high-frequency signal generator 3 (CW interference signal) are used in combination. When executing an intermodulation characteristics test, it must be externally added with a CW signal (high-frequency signal generator 2) with 600-kHz offset that is generated by another CW signal generator.

***Note*:**

To use this combination file, Combination of Baseband Signal (option) is required.

3.6.1 Frame configuration

Each PHS frame is composed of four uplink slots and four downlink slots (eight slots in total), and data is generated cyclically based on one PHS frame. Only Slot 1 is transmitted, and subsequent Slots 2 through 4 are not transmitted (transmission off). A PN9 pseudo random pattern in the TCH field of each slot is independent within the slot has continuity between frames.

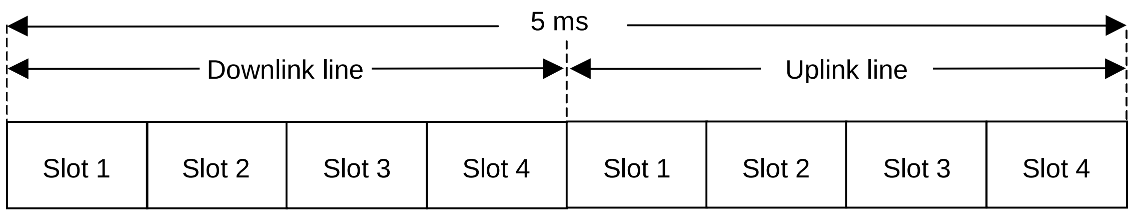


Figure 3.6.1-1 PHS frame configuration

In a waveform pattern other than PI_4_DQPSK_PN9, PI_4_DQPSK_PN15 and PI_4_DQPSK_ALL0, a communication channel is allocated to uplink or downlink Slot 1. Other slots are burst off output.

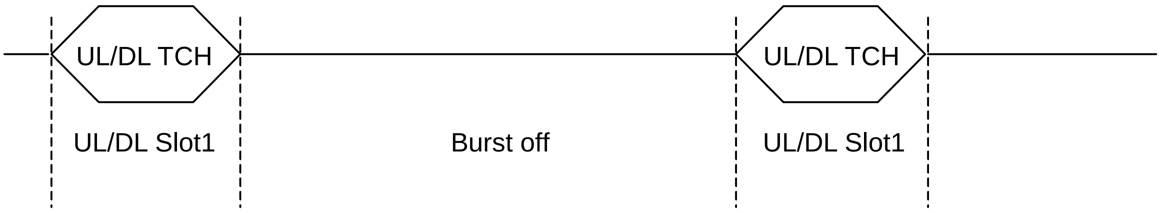


Figure 3.6.1-2 Output of waveform pattern other than PI_4_DQPSK_PN9/15/ALL0

3.6.2 Slot configuration

There are two types of slot configurations: downlink traffic channel and uplink traffic channel. The scramble function is always Off.

Uplink/downlink traffic channel

R 4	S S 2	P R 6	UW 16	CI 4	SA 16	TCH 160	CR C 16	G 16

R:	Ramp time for transient response	0_H (4 bits)
SS:	Start symbol	2_H (2 bits)
PR	Preamble	19_H (6 bits)
UW:	Sync word	Uplink = $E149_H$ (16 bits) Downlink = $3D4C_H$ (16 bits)
CI:	Channel identification	0_H (4 bits)
SA:	SACCH	8000_H (16 bits)
TCH:	Information channel	PN9 pseudo random pattern independent in each slot (PN pattern is continuous in TCH of a slot).
CRC:	Cyclic redundancy check code	CRC bits for CI, SA, TCH
G:	Guard time for transient response	0000_H (16 bits)

3.7 GSM Waveform Pattern

As the GSM waveform pattern, waveform patterns for uplink/downlink are provided as shown in Table 3.7-1.

Table 3.7-1 List of GSM waveform patterns

Waveform Pattern Name	Uplink/Downlink	Data	Output Slot
Package name: GSM			
GMSK_PN9	Uplink/Downlink	PN9 *1	–
8PSK_PN9	Uplink/Downlink		–
GMSK_TN0	Uplink/Downlink	PN9 *2	TN0
8PSK_TN0	Uplink/Downlink		TN0
NB_GMSK	Uplink/Downlink	PN9 *3	TN0
NB_ALL_GMSK	Uplink/Downlink		All slots
NB_8PSK	Uplink/Downlink		TN0
NB_ALL_8PSK	Uplink/Downlink		All slots
TCH_FS	Uplink/Downlink	PN9 *4	TN0
CS-1_1SLOT	Uplink/Downlink		TN0
CS-4_1SLOT	Uplink/Downlink		TN0
DL_MCS-1_1SLOT	Downlink		TN0
UL_MCS-1_1SLOT	Uplink		TN0
DL_MCS-5_1SLOT	Downlink		TN0
UL_MCS-5_1SLOT	Uplink		TN0
DL_MCS-9_1SLOT	Downlink		TN0
UL_MCS-9_1SLOT	Uplink		TN0
DL_MCS-9_4SLOT*5	Downlink		TN0, 1, 2, 3
UL_MCS-9_4SLOT*5	Uplink		TN0, 1, 2, 3

*1: PN9 data is inserted to all the non-slot format fields.
*2: PN9 data is inserted to all the fields in a slot except the guard.
*3: PN9 data is inserted to the encrypted bit fields of normal burst.
*4: A bit sequence generated by channel-coding the PN9 data is inserted to the encrypted bit fields of normal burst.
*5: To use this waveform pattern, ARB Memory Upgrade 256 Msample (option) or ARB Memory Upgrade 1024 Msample (option), is required.

When outputting each GSM waveform pattern, marker signal (Marker 1, Marker 2) as outlined in the Table 3.7-2 is output from Marker1 Output connector of MG3710A rear panel or from AUX connector. For details of output connector setting, refer to 7.4.2 “Route Output Connectors” in MG3710A Vector Signal Generator Operation Manual (Mainframe).

Table 3.7-2 Marker output data and IQ output level

Marker Signal	Output Data
Marker 1	Frame Clock
Marker 2	RF Gate
Marker 3	Multi-Frame Clock

3.7.1 Details of each pattern

♦ GMSK_PN9, PSK_PN9

PN9 data which doesn't have slot format is inserted.

♦ GMSK_TN0, 8PSK_TN0

PN9 data is inserted to all the fields in a slot except the guard field. The PN9 data in each slot has continuity.

♦ NB_GMSK, NB_ALL_GMSK, NB_8PSK, NB_ALL_8PSK

PN9 data is inserted to the encrypted bit fields of normal burst. The PN9 data in each slot has continuity.

♦ TCH_FS

Supports Speech channel at full rate (TCH/FS) prescribed in 3GPP TS05.03 Section 3.1.
The table below shows channel coding parameters:

Type of Channel	Bits/Block Data + Parity + Tail1	Convolutional Code Rate	Coded Bits per Block	Interleaving Depth
TCH/FS			456	8
class I	182 + 3 + 4	1/2	378	
class II	78 + 0 + 0	–	78	

♦ CS-1(4)_1SLOT

Supports Packet data block type 1 (CS-4), 4 (CS-1) of GPRS PDTCH prescribed in 3GPP TS05.03 Section 5.1.
The table below shows channel coding parameters:

Scheme	Code Rate	USF	Pre-coded USF	Radio Block excl. USF and BCS	BCS	Tail	Coded Bits	Punctured Bits
CS-1	1/2	3	3	181	40	4	456	0
CS-4	1	3	12	428	16	–	456	–

♦ DL(UL)_MCS-1(5, 9)_1SLOT(_4SLOT)

Supports Packet data block type 5 (MCS-1), 9 (MCS-5), and 13 (MCS-9) of EGPRS PDTCH prescribed in 3GPP TS05.03 Section 5.1.

The table below shows channel coding parameters:

<table>
<tr><th>Scheme</th><th>Code Rate</th><th>Header Code Rate (Note)</th><th>Modulation</th><th>RLC Blocks per Radio Block (20 ms)</th><th>Raw Data within One Radio Block</th><th>Family</th><th>BCS</th><th>Tail Payload</th><th>HCS</th><th>Data Rate kb/s</th></tr>
<tr><td>MCS-9</td><td>1.0</td><td>0.36</td><td rowspan="2">8PSK</td><td>2</td><td>2x592</td><td>A</td><td>2x12</td><td>2x6</td><td rowspan="3">8</td><td>59.2</td></tr>
<tr><td>MCS-5</td><td>0.37</td><td>1/3</td><td>1</td><td>448</td><td>B</td><td rowspan="2">12</td><td rowspan="2">6</td><td>22.4</td></tr>
<tr><td>MCS-1</td><td>0.53</td><td>0.53</td><td>GMSK</td><td>1</td><td>176</td><td>C</td><td>8.8</td></tr>
</table>

Note:

The Header data is all “0.”

3.7.2 Frame configuration

Each frame is composed of eight slots. TCH/FS consist of 26 multiframes, and other channels consist of 52 multiframes.

3.7.3 Slot configuration

♦ GMSK_TN0 and 8PSK_TN0 consist of the data field and guard field only as shown in the figures below:

PN 148	G 8.25

Unit: bit

PN:	Data	PN9 pseudo random pattern (continuous between transmitted slots)
G:	Guard bit	FF_H

PN 444	G 24.75

Unit: bit

PN:	Data	PN9 pseudo random pattern (continuous between transmitted slots)
G:	Guard bit	FF_H

♦ The slot configuration for those other than GMSK_PN9, 8PSK_PN9, GMSK_TN0, and 8PSK_TN0 is normal burst as shown in the figure below:

Normal burst (GMSK)

T 3	E 57	S 1	TSC 26	S 1	E 57	T 3	G 8.2 5

Unit: bit

T:	Tail bit	0_H (4 bits)
E:	Encrypted bit	Channel-coded (see Note) PN9 pseudo random pattern (continuous between transmitted slots)
S:	Stealing bit	Steal flag
TSC:	Training sequence bit	097 0897_H
T:	Tail bit	0_H (4 bits)
G:	Guard bit	FF_H

Normal burst (8PSK)

T1 9	E 174	TSC 78	E 174	T 2 9	G 24. 75

Unit: bit

T1:	Tail bit	$1FF_H$ (9 bits)
E:	Encrypted bit	Channel-coded (see Note) PN9 pseudo random pattern (continuous between transmitted slots)
TSC:	Training sequence bit	3F3F 9E29 FFF3 FF3F $9E49_H$
T2:	Tail bit	$1FF_H$ (9 bits)
G:	Guard bit	FF_H

Note:

When the waveform pattern is NB, PN9 data that has not been channel-coded is inserted directly.

3.8 CDMA2000 1X Waveform Pattern

As the CDMA2000 1X waveform pattern, waveform patterns shown in Table 3.8-1 are provided.

Table 3.8-1 List of CDMA2000 1X waveform patterns

Waveform Pattern Name	Supported System	Frame Coding	Output Slot
Package name: CDMA2000			
RVS_RC1_FCH	cdma2000 1xRTT RC1 Reverse	Applicable	FCH 9.6 kbps
RVS_RC2_FCH	cdma2000 1xRTT RC2 Reverse	Applicable	FCH 14.4 kbps
RVS_RC3_FCH	cdma2000 1xRTT RC3 Reverse	Applicable	PICH FCH 9.6 kbps
RVS_RC3_FCH_SCH	cdma2000 1xRTT RC3 Reverse	Applicable	PICH FCH 9.6 kbps SCH 9.6 kbps
RVS_RC3_DCCH	cdma2000 1xRTT RC3 Reverse	Applicable	PICH DCCH 9.6 kbps
RVS_RC4_FCH	cdma2000 1xRTT RC4 Reverse	Applicable	PICH FCH 14.4 kbps
FWD_RC1-2_9channel	cdma2000 1xRTT RC1, RC2 Forward	Spreading only	PICH, SyncCH, PagingCH, FCH 19.2 ksps x 6
FWD_RC3-5_9channel	cdma2000 1xRTT RC3, RC4, RC5 Forward	Spreading only	PICH, SyncCH, PagingCH, FCH 38.4 ksps x 6

When outputting each CDMA2000 1X waveform pattern, marker signal (Marker 1, Marker 2, Marker 3) as outlined in the Table 3.8-2 is output from Marker1 Output connector of MG3710A rear panel or from AUX connector. For details of output connector setting, refer to 7.4.2 “Route Output Connectors” in MG3710A Vector Signal Generator Operation Manual (Mainframe).

Table 3.8-2 Marker output data and IQ output level

Marker Signal	Output Data
Marker 1	Frame Clock
Marker 2	RF Gate
Marker 3	Symbol Clock
AWGN addition (Note)	Enable

3.8.1 1xRTT Reverse RC1 (RVS_RC1_FCH)

When this waveform pattern is selected, a frame-coded R-FCH signal accommodating 1xRTT Reverse RC1 is output. The frame coding and IQ modulation conform to 3GPP2 C.S0002-C-1. Table 3.8.1-1 shows the output signal parameter.

Table 3.8.1-1 R-FCH (Reverse Fundamental Channel)

	Data Rate	Data
R-FCH	9.6 kbps	PN9fix*

The frame coding illustrated in the functional diagram of Figure 3.8.1-2 is executed for the signals that are output by selecting this waveform pattern. The frame coding is continuously executed for four frames (it takes about 20 ms to output one frame), and a 4-frame length signal pattern obtained by executing the frame coding is output repeatedly. Since the total length of three cycles of I Channel PN Sequence and Q Channel PN Sequence, which are used for the short-code spreading, is 80 ms and equals to the length of four frames, the short code holds the continuity during signal output. Therefore, the signals output by selecting this waveform pattern are usable for modulation accuracy measurement and FER (Frame Error Rate) measurement with CRC. The long-code spreading is not processed.

Figure 3.8.1-1 shows the assignment of bit sequences before executing convolutional coding.

PN9fix* (172 bits)	Frame Quality Indicator (12 bits)	Encoder Tail Bits (“00000000”)

Figure 3.8.1-1 Frame configuration of waveform pattern RVS_RC1_FCH

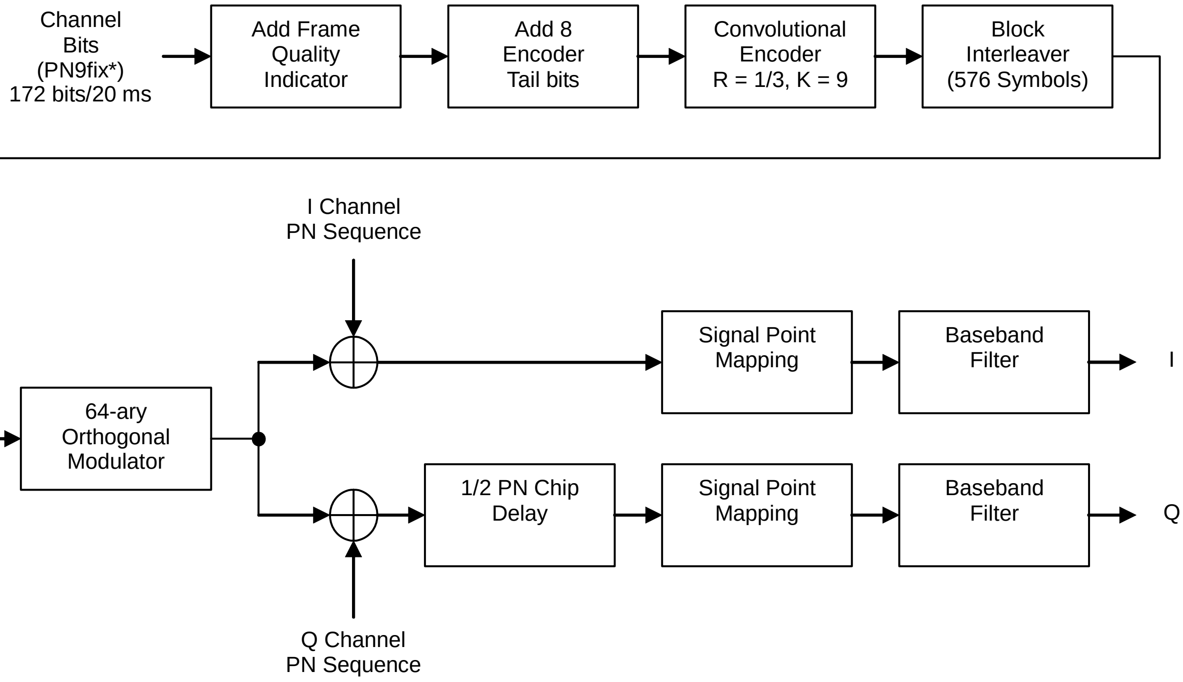


Figure 3.8.1-2 Signal generation block diagram of waveform pattern RVS_RC1_FCH

*: 4-frame length data, which is generated by initializing the PN9 generator for each 4 frames, is output repeatedly as shown in Figure 3.8.1-3 below. This is why the continuity of PN9fix is held within the four frames, but the continuity with other four frames is lost.

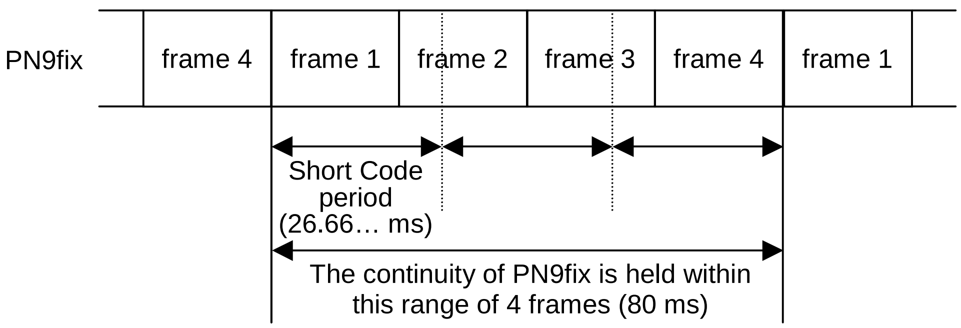


Figure 3.8.1-3 PN9fix data and short code

3.8.2 1xRTT Reverse RC2 (RVS_RC2_FCH)

When this waveform pattern is selected, a frame-coded R-FCH signal accommodating 1xRTT Reverse RC2 is output. The frame coding and IQ modulation conform to 3GPP2 C.S0002-C-1. Table 3.8.2-1 shows the output signal parameter.

Table 3.8.2-1 R-FCH (Reverse Fundamental Channel)

	Data Rate	Data
R-FCH	14.4 kbps	PN9fix*

The frame coding illustrated in the functional diagram of Figure 3.8.2-2 is executed for the signals that are output by selecting this waveform pattern. The frame coding is continuously executed for four frames (it takes about 20 ms to output one frame), and a 4-frame length signal pattern obtained by executing the frame coding is output repeatedly. Since the total length of three cycles of I Channel PN Sequence and Q Channel PN Sequence, which are used for the short-code spreading, is 80 ms and equals to the length of four frames, the short code holds the continuity during signal output. Therefore, the signals output by selecting this waveform pattern are usable for modulation accuracy measurement and FER (Frame Error Rate) measurement with CRC. The long-code spreading is not processed.

Figure 3.8.2-1 shows the assignment of bit sequences before executing convolutional coding.

Erasure Indicator Bit ("0")	PN9fix* (267 bits)	Frame Quality Indicator (12 bits)	Encoder Tail Bits ("00000000")

Figure 3.8.2-1 Frame configuration of waveform pattern RVS_RC2_FCH

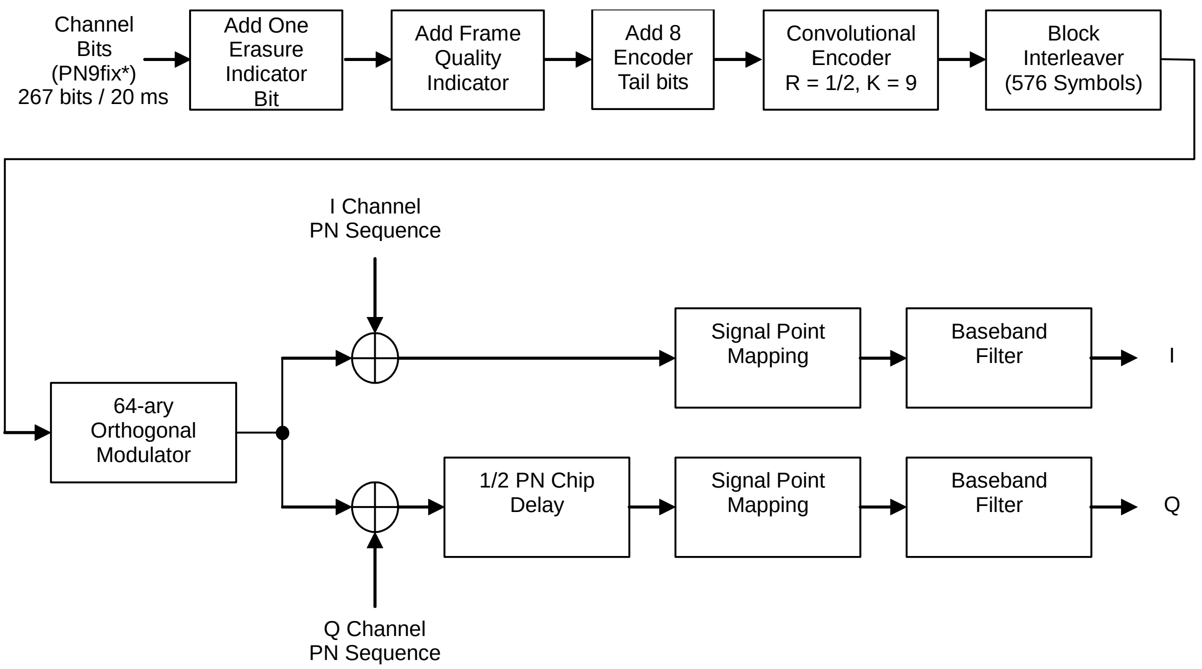


Figure 3.8.2-2 Signal generation block diagram of waveform pattern RVS_RC2_FCH

*: 4-frame length data is output repeatedly because the PN9 generator is initialized for each 4 frames. This is why the continuity of PN9fix is held within the four frames, but the continuity with other four frames is lost.
See Figure 3.8.1-3 "PN9fix data and short code" in Section 3.8.1 for details.

3.8.3 1xRTT Reverse RC3 (1) (RVS_RC3_FCH)

When this waveform pattern is selected, a frame-coded multiplexed signal accommodating 1xRTT Reverse RC3 is output. The frame coding and IQ modulation conform to 3GPP2 C.S0002-C-1. The multiplexed channels are R-PICH and R-FCH. Table 3.8.3-1 shows the output signal parameters.

Table 3.8.3-1 R-PICH (Reverse Pilot Channel), R-FCH (Reverse Fundamental Channel)

	Walsh Code	Code Power	Data Rate	Data
R-PICH	0	–5.278 dB	N/A	All “0”
R-FCH	4	–1.528 dB	9.6 kbps	PN9fix*

The frame coding illustrated in the functional diagrams of Figs. 3.8.3-2 and 3.8.3-3 is executed for the signals that are output by selecting this waveform pattern. The frame coding is continuously executed for four frames (it takes about 20 ms to output one frame), and a 4-frame length signal pattern obtained by executing the frame coding is output repeatedly. Since the total length of three cycles of I Channel PN Sequence and Q Channel PN Sequence, which are used for the short-code spreading, is 80 ms and equals to the length of four frames, the short code holds the continuity during signal output. Therefore, the signals output by selecting this waveform pattern are usable for modulation accuracy measurement and FER (Frame Error Rate) measurement with CRC. The long-code spreading is not processed.

Figure 3.8.3-1 shows the assignment of bit sequences before executing convolutional coding.

PN9fix* (172 bits)	Frame Quality Indicator (12 bits)	Encoder Tail Bits (“00000000”)

Figure 3.8.3-1 Traffic channel frame configuration of waveform pattern RVS_RC3_FCH

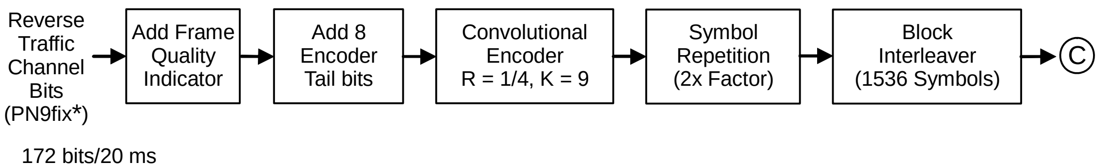


Figure 3.8.3-2 Signal generation block diagram of waveform pattern RVS_RC3_FCH (1/2)

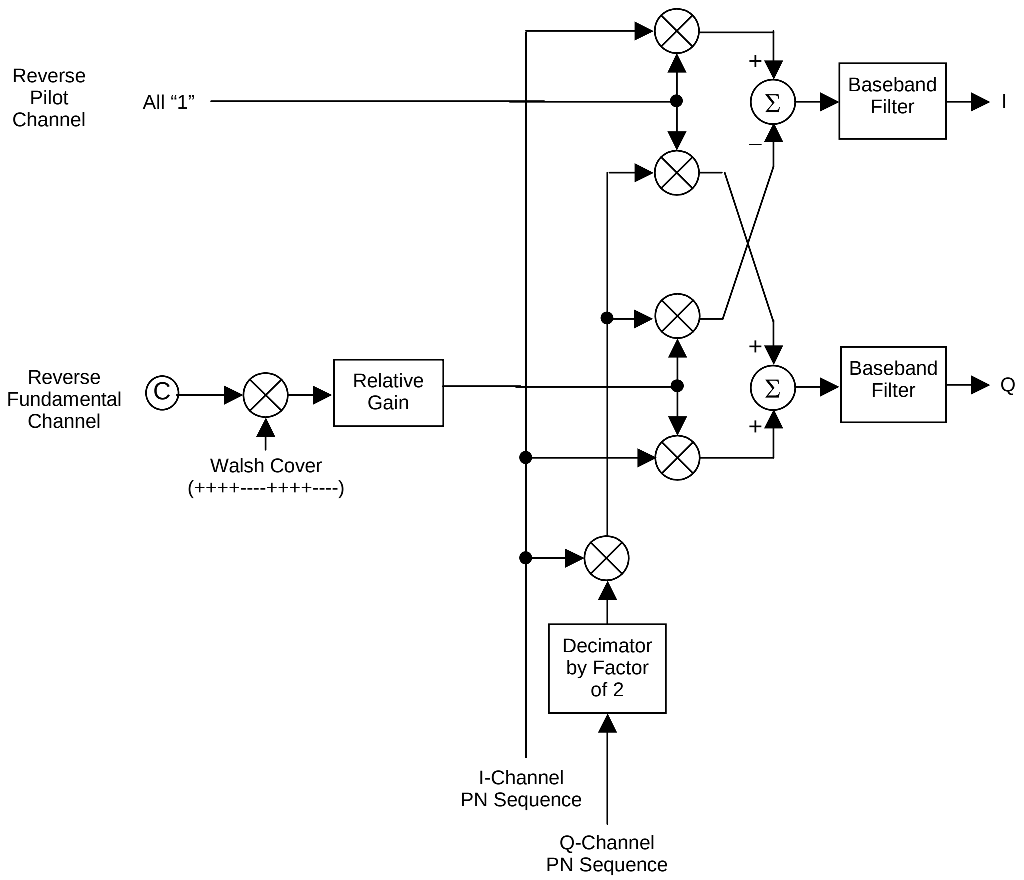


Figure 3.8.3-3 Signal generation block diagram of waveform pattern RVS_RC3_FCH (2/2)

Note:

Binary numbers “0” and “1” are replaced by 1 and –1, respectively.

*: 4-frame length data is output repeatedly because the PN9 generator is initialized for each 4 frames. This is why the continuity of PN9fix is held within the four frames, but the continuity with other four frames is lost.
See Figure 3.8.1-3 “PN9fix data and short code” in Section 3.8.1 for details.

3.8.4 1xRTT Reverse RC3 (2) (RVS_RC3_FCH_SCH)

When this waveform pattern is selected, a frame-coded multiplexed signal accommodating 1xRTT Reverse RC3 is output. The frame coding and IQ modulation conform to 3GPP2 C.S0002-C-1. The multiplexed channels are R-PICH, R-FCH, and R-SCH. Table 3.8.4-1 shows the output signal parameters.

Table 3.8.4-1 R-PICH (Reverse Pilot Channel), R-FCH (Reverse Fundamental Channel), R-SCH (Reverse Supplemental Channel)

	Walsh Code	Code Power	Data Rate	Data
R-PICH	0	−7.5912 dB	N/A	All “0”
R-FCH	4	−3.8412 dB	9.6 kbps	PN9fix*
R-SCH	2	−3.8412 dB	9.6 kbps	PN9fix*

The frame coding illustrated in the functional diagrams of Figs. 3.6.4-2 and 3.6.4-3 is executed for the signals that are output by selecting this waveform pattern. The frame coding is continuously executed for four frames (it takes about 20 ms to output one frame), and a 4-frame length signal pattern obtained by executing the frame coding is output repeatedly. Since the total length of three cycles of I Channel PN Sequence and Q Channel PN Sequence, which are used for the short-code spreading, is 80 ms and equals to the length of four frames, the short code holds the continuity during signal output. Therefore, the signals output by selecting this waveform pattern are usable for modulation accuracy measurement and FER (Frame Error Rate) measurement with CRC. The long-code spreading is not processed.

Figure 3.8.4-1 shows the assignment of bit sequences before executing convolutional coding.

PN9fix* (172 bits)	Frame Quality Indicator (12 bits)	Encoder Tail Bits (“00000000”)

Figure 3.8.4-1 Traffic channel frame configuration of waveform pattern RVS_RC3_FCH_SCH

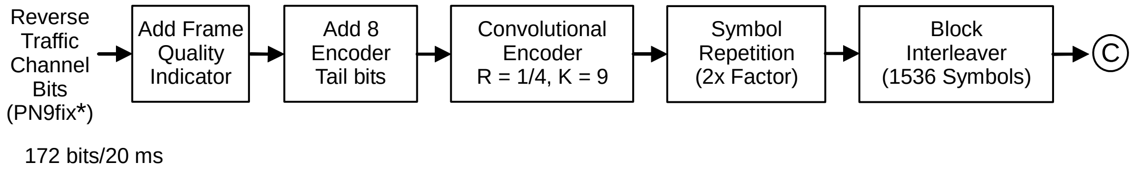


Figure 3.8.4-2 Signal generation block diagram of waveform pattern RVS_RC3_FCH_SCH (1/2)

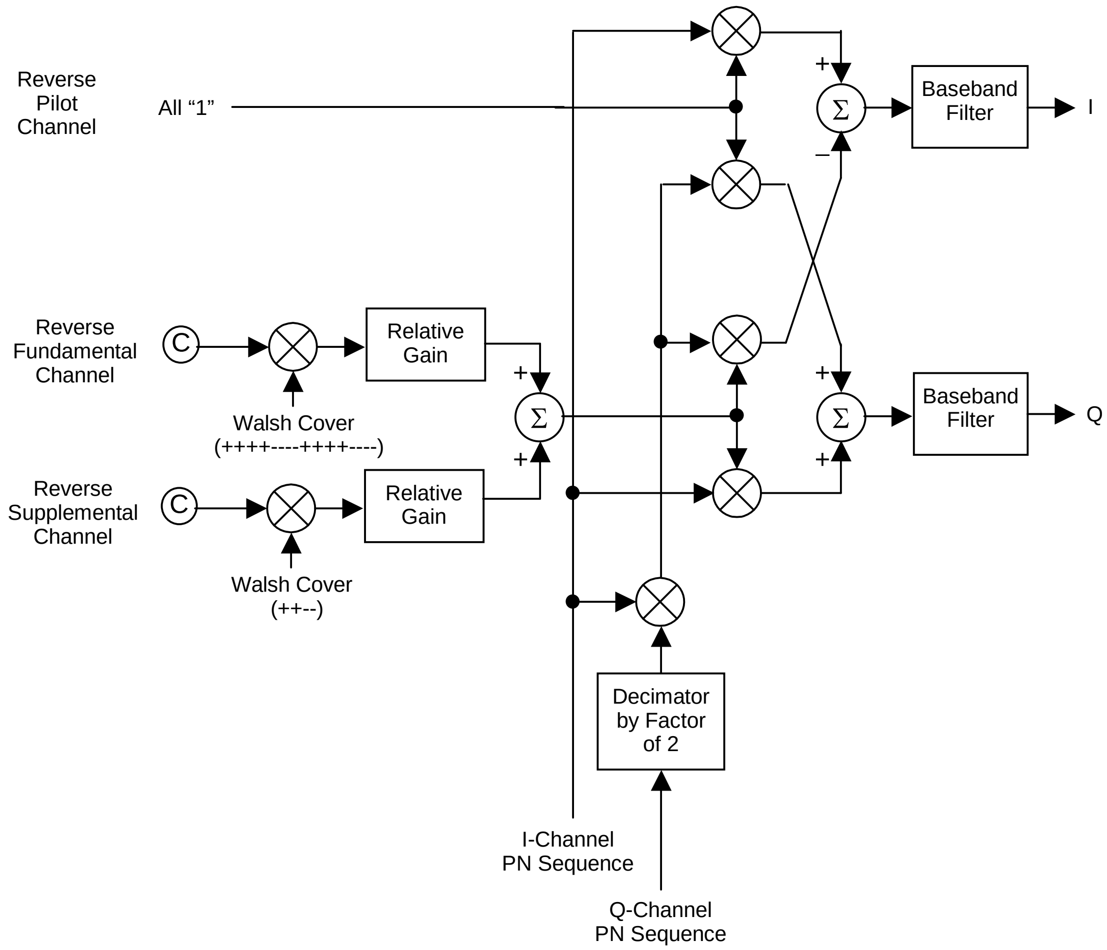


Figure 3.8.4-3 Signal generation block diagram of waveform pattern RVS_RC3_FCH_SCH (2/2)

Note:

Binary numbers “0” and “1” are replaced by 1 and –1, respectively.

*: 4-frame length data is output repeatedly because the PN9 generator is initialized for each 4 frames. This is why the continuity of PN9fix is held within the four frames, but the continuity with other four frames is lost.
See Figure 3.8.1-3 “PN9fix data and short code” in Section 3.8.1 for details.

3.8.5 1xRTT Reverse RC3 (3) (RVS_RC3_DCCH)

When this waveform pattern is selected, a frame-coded multiplexed signal accommodating 1xRTT Reverse RC3 is output. The frame coding and IQ modulation conform to 3GPP2 C.S0002-C-1. The multiplexed channels are R-PICH and R-DCCH. Table 3.8.5-1 shows the output signal parameters.

Table 3.8.5-1 R-PICH (Reverse Pilot Channel), R-DCCH (Reverse Dedicated Control Channel)

	Walsh Code	Code Power	Data Rate	Data
R-PICH	0	–5.278 dB	N/A	All “0”
R-DCCH	8	–1.528 dB	9.6 kbps	PN9fix*

The frame coding illustrated in the functional diagrams of Figs. 3.8.5-2 and 3.8.5-3 is executed for the signals that are output by selecting this waveform pattern. The frame coding is continuously executed for four frames (it takes about 20 ms to output one frame), and a 4-frame length signal pattern obtained by executing the frame coding is output repeatedly. Since the total length of three cycles of I Channel PN Sequence and Q Channel PN Sequence, which are used for the short-code spreading, is 80 ms and equals to the length of four frames, the short code holds the continuity during signal output. Therefore, the signals output by selecting this waveform pattern are usable for modulation accuracy measurement and FER (Frame Error Rate) measurement with CRC. The long-code spreading is not processed.

Figure 3.8.5-1 shows the assignment of bit sequences before executing convolutional coding.

PN9fix* (172 bits)	Frame Quality Indicator (12 bits)	Encoder Tail Bits (“00000000”)

Figure 3.8.5-1 Traffic channel frame configuration of waveform pattern RVS_RC3_DCCH

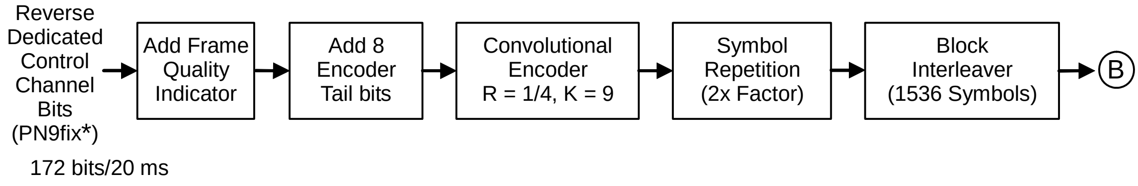


Figure 3.8.5-2 Signal generation block diagram of waveform pattern RVS_RC3_DCCH (1/2)

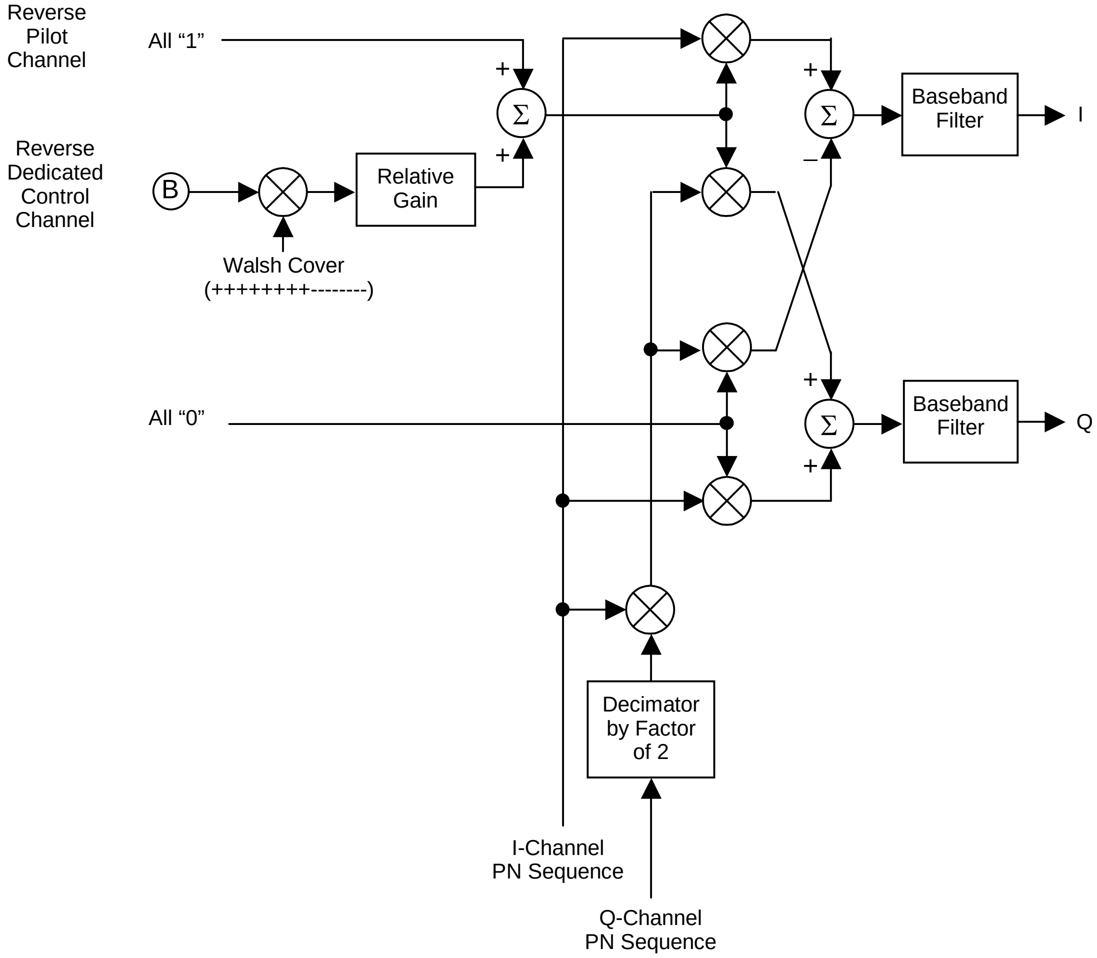


Figure 3.8.5-3 Signal generation block diagram of waveform pattern RVS_RC3_DCCH (2/2)

Note:

Binary numbers “0” and “1” are replaced by 1 and –1, respectively.

*: 4-frame length data is output repeatedly because the PN9 generator is initialized for each 4 frames. This is why the continuity of PN9fix is held within the four frames, but the continuity with other four frames is lost.
See Figure 3.8.1-3 “PN9fix data and short code” in Section 3.8.1 for details.

3.8.6 1xRTT Reverse RC4 (RVS_RC4_FCH)

When this waveform pattern is selected, a frame-coded multiplexed signal accommodating 1xRTT Reverse RC4 is output. The frame coding and IQ modulation conform to 3GPP2 C.S0002-C-1. The multiplexed channels are R-PICH and R-FCH. Table 3.8.6-1 shows the output signal parameters.

Table 3.8.6-1 R-PICH (Reverse Pilot Channel), R-FCH (Reverse Fundamental Channel)

	Walsh Code	Code Power	Data Rate	Data
R-PICH	0	–5.278 dB	N/A	All “0”
R-FCH	4	–1.528 dB	14.4 kbps	PN9fix*

The frame coding illustrated in the functional diagrams of Figs. 3.8.6-2 and 3.8.6-3 is executed for the signals that are output by selecting this waveform pattern. The frame coding is continuously executed for four frames (it takes about 20 ms to output one frame), and a 4-frame length signal pattern obtained by executing the frame coding is output repeatedly. Since the total length of three cycles of I Channel PN Sequence and Q Channel PN Sequence, which are used for the short-code spreading, is 80 ms and equals to the length of four frames, the short code holds the continuity during signal output. Therefore, the signals output by selecting this waveform pattern are usable for modulation accuracy measurement and FER (Frame Error Rate) measurement with CRC. The long-code spreading is not processed.

Figure 3.8.6-1 shows the assignment of bit sequences before executing convolutional coding.

Reserved Bit (“0”)	PN9fix* (267 bits)	Frame Quality Indicator (12 bits)	Encoder Tail Bits (“00000000”)

Figure 3.8.6-1 Traffic channel frame configuration of waveform pattern RVS_RC4_FCH

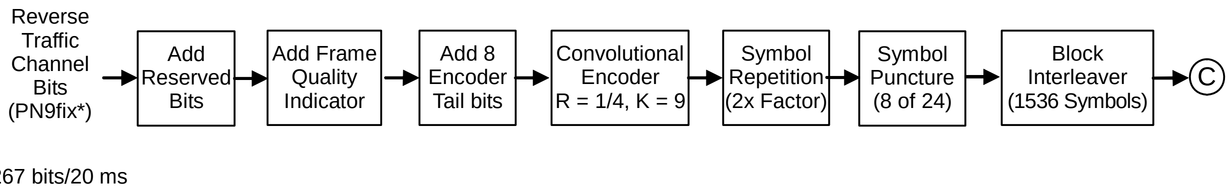


Figure 3.8.6-2 Signal generation block diagram of waveform pattern RVS_RC4_FCH (1/2)

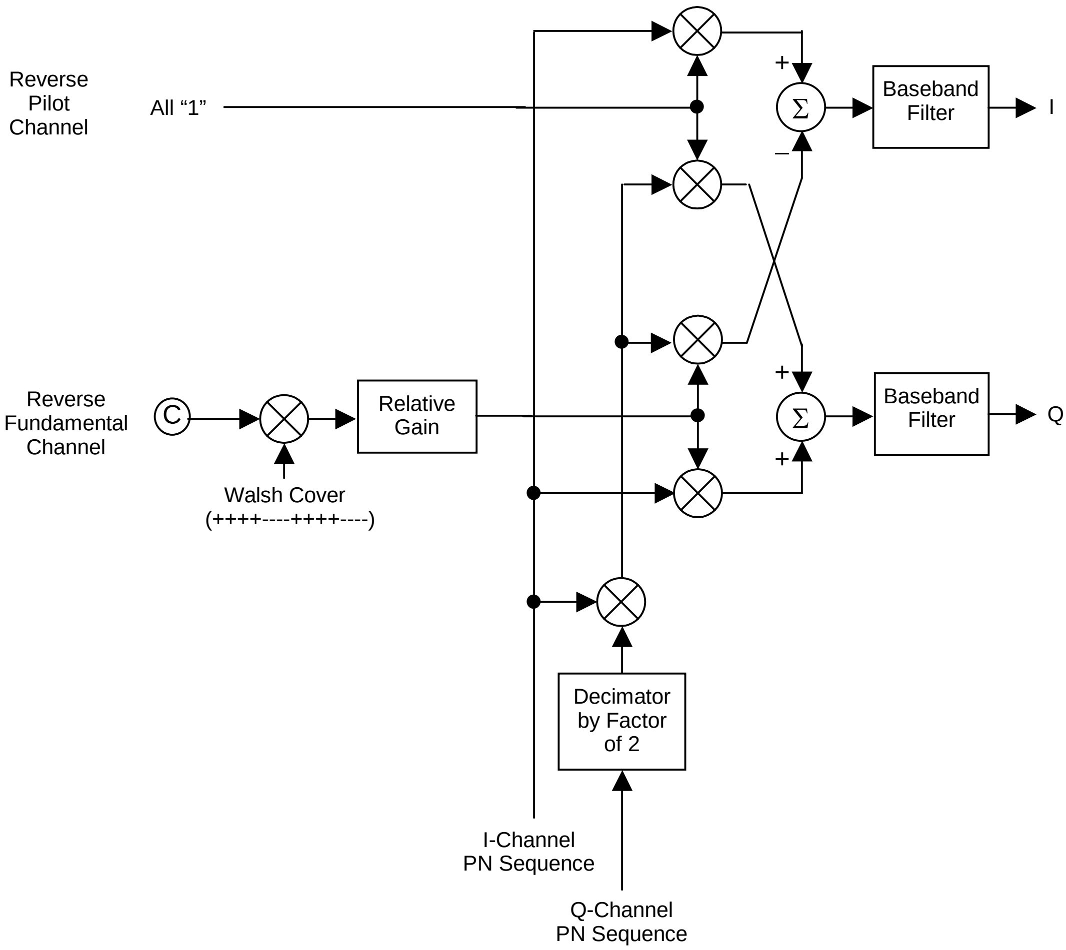


Figure 3.8.6-3 Signal generation block diagram of waveform pattern RVS_RC4_FCH (2/2)

Note:

Binary numbers “0” and “1” are replaced by 1 and –1, respectively.

*: 4-frame length data is output repeatedly because the PN9 generator is initialized for each 4 frames. This is why the continuity of PN9fix is held within the four frames, but the continuity with other four frames is lost.
See Figure 3.8.1-3 “PN9fix data and short code” in Section 3.8.1 for details.

3.8.7 1xRTT Forward RC1, 2 (FWD_RC1-2 9channel)

When this waveform pattern is selected, a multiplexed signal accommodating 1xRTT Forward RC1, RC2 that conform to 3GPP2 C.S0002-C-1 is output. The multiplexed channels are F-PICH, F-SyncCH, PagingCH, and F-FCH x 6 (data sequence generated by spreading six symbol data sequences according to spreading code of Walsh Code 8, 9, …, 13). Table 3.8.7-1 shows the multiplexed channel parameters.

Table 3.8.7-1 F-PICH (Forward Pilot Channel), F-SyncCH (Forward Sync Channel), PagingCH (Paging Channel), F-FCH (Forward Fundamental Channel)

	Walsh Code	Code Power	Symbol Rate	Symbol Data
F-PICH	0	–7.0 dB	N/A	All “0”
F-SyncCH	32	–13.3 dB	4.8 ksps	PN9fix*
PagingCH	1	–7.3 dB	19.2 ksps	PN9fix*
F-FCH x 6	8 to 13	–10.3 dB	19.2 ksps	PN9fix*

The processing illustrated in the functional diagram of Figure 3.8.7-1 is executed for the signals that are output by selecting this waveform pattern. The convolutional coding and interleaving are not processed. This functional diagram should be applied to each channel, and the symbol data of the channels are separately processed as indicated in this functional diagram and then added each other. The frame coding is continuously executed for four frames (it takes about 20 ms to output one frame), and a 4-frame length signal pattern obtained by executing the frame coding is output repeatedly. Since the total length of three cycles of I Channel PN Sequence and Q Channel PN Sequence, which are used for the short-code spreading, is 80 ms and equals to the length of four frames, the short code holds the continuity during signal output. Therefore, the signals output by selecting this waveform pattern are usable for modulation accuracy measurement and FER (Frame Error Rate) measurement with CRC. The long-code scrambling and PCB Mux are not processed.

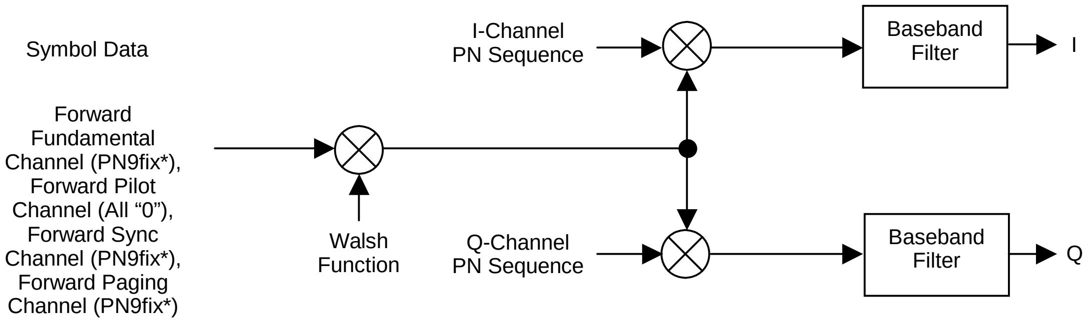


Figure 3.8.7-1 Signal generation block diagram of waveform pattern FWD_RC1-2 9channel

Note:

Binary numbers “0” and “1” are replaced by 1 and –1, respectively.

*: 4-frame length data is output repeatedly because the PN9 generator is initialized for each 4 frames. This is why the continuity of PN9fix is held within the four frames, but the continuity with other four frames is lost.
See Figure 3.8.1-3 “PN9fix data and short code” in Section 3.8.1 for details.

3.8.8 1xRTT Forward RC3, 4, 5 (FWD_RC3-5 9channel)

When this waveform pattern is selected, a multiplexed signal accommodating 1xRTT Forward RC3, RC4, RC5 that conform to 3GPP2 C.S0002-C-1 is output. The multiplexed channels are F-PICH, F-SyncCH, PagingCH, and F-FCH x 6 (data sequence generated by spreading six symbol data sequences according to spreading code of Walsh Code8, 9, …, 13). Table 3.8.8-1 shows the multiplexed channel parameters.

Table 3.8.8-1 F-PICH (Forward Pilot Channel), F-SyncCH (Forward Sync Channel), PagingCH (Paging Channel), F-FCH (Forward Fundamental Channel)

	Walsh Code	Code Power	Symbol Rate	Symbol Data
F-PICH	0	−7.0 dB	N/A	All “0”
F-SyncCH	32	−13.3 dB	4.8 ksps	PN9fix*
PagingCH	1	−7.3 dB	19.2 ksps	PN9fix*
F-FCH x 6	8 to 13	−10.3 dB	38.4 ksps	PN9fix*

The processing illustrated in the functional diagrams of Figs. 3.8.8-1 and 3.8.8-2 is executed for the signals that are output by selecting this waveform pattern. The convolutional coding and interleaving are not processed. This functional diagram should be applied to each channel, and the symbol data of the channels are separately processed as indicated in this functional diagram and then added each other. The frame coding is continuously executed for four frames (it takes about 20 ms to output one frame), and a 4-frame length signal pattern obtained by executing the frame coding is output repeatedly. Since the total length of three cycles of I Channel PN Sequence and Q Channel PN Sequence, which are used for the short-code spreading, is 80 ms and equals to the length of four frames, the short code holds the continuity during signal output. Therefore, the signals output by selecting this waveform pattern are usable for modulation accuracy measurement and FER (Frame Error Rate) measurement with CRC. The long-code scrambling and PCB Mux are not processed.

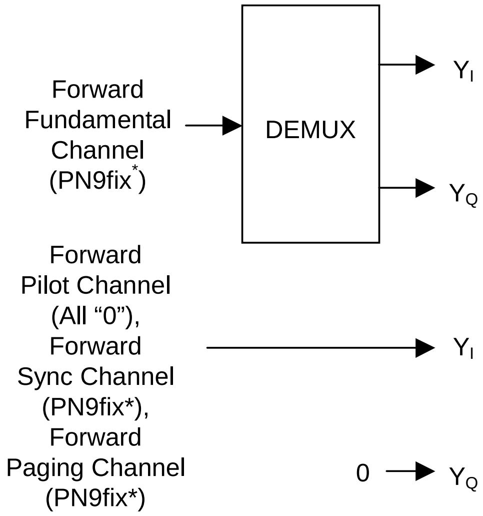


Figure 3.8.8-1 Signal generation block diagram of waveform pattern FWD_RC3-5 9channel (1/2)

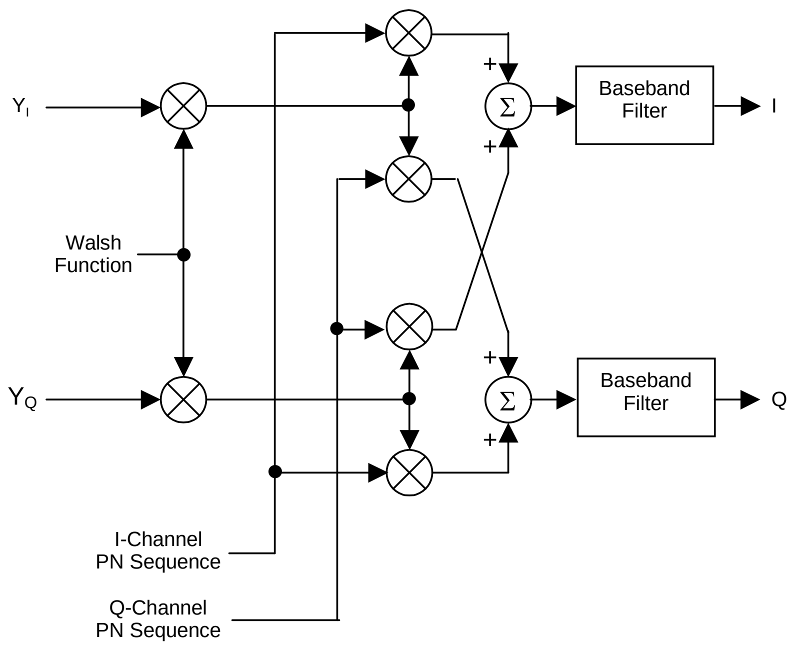


Figure 3.8.8-2 Signal generation block diagram of waveform pattern FWD_RC3-5 9channel (2/2)

Note:

Binary numbers "0" and "1" are replaced by 1 and –1, respectively.

*: 4-frame length data is output repeatedly because the PN9 generator is initialized for each 4 frames. This is why the continuity of PN9fix is held within the four frames, but the continuity with other four frames is lost. See Figure 3.8.1-3 "PN9fix data and short code" in Section 3.8.1 for details.

3.9 CDMA2000 1xEV-DO Waveform Pattern

As the CDMA2000 1xEV-DO waveform pattern, the following waveform patterns are provided.

FWD_38_4_16slot/…/FWD_2457_6_1slot
When these waveform patterns are selected, CDMA2000 1xEV-DO forward modulated signal for which channel coding, TDM, and IQ mapping are executed according to 3GPP2 C.S0024 is output.

FWD_Idle
When this waveform pattern is selected, CDMA2000 1xEV-DO forward idle slot modulated signal for which TDM and IQ mapping are executed according to 3GPP2 C.S0024 is output.

RVS_9_6_kbps_RX/…/RVS_153_6_kbps_RX
When these waveform patterns are selected, CDMA2000 1xEV-DO reverse modulated signal for which channel coding and IQ mapping are executed according to 3GPP2 C.S0024 is output.

Table 3.9-1 lists the CDMA2000 1xEV-DO waveform patterns.

Table 3.9-1 List of CDMA2000 1xEV-DO waveform patterns (1/2)

1xEV-DO Waveform Pattern	Supported System	Baseband Filter	Data
Package name: CDMA2000_1xEV-DO			
FWD_38_4kbps_16slot	CDMA2000 1xEV-DO Forward	IS-95SPEC+EQ	PN15fix*
FWD_76_8kbps_8slot	CDMA2000 1xEV-DO Forward	IS-95SPEC+EQ	PN15fix*
FWD_153_6kbps_4slot	CDMA2000 1xEV-DO Forward	IS-95SPEC+EQ	PN15fix*
FWD_307_2kbps_2slot	CDMA2000 1xEV-DO Forward	IS-95SPEC+EQ	PN15fix*
FWD_614_4kbps_1slot	CDMA2000 1xEV-DO Forward	IS-95SPEC+EQ	PN15fix*
FWD_307_2kbps_4slot	CDMA2000 1xEV-DO Forward	IS-95SPEC+EQ	PN15fix*
FWD_614_4kbps_2slot	CDMA2000 1xEV-DO Forward	IS-95SPEC+EQ	PN15fix*
FWD_1228_8kbps_1slot	CDMA2000 1xEV-DO Forward	IS-95SPEC+EQ	PN15fix*
FWD_921_6kbps_2slot	CDMA2000 1xEV-DO Forward	IS-95SPEC+EQ	PN15fix*
FWD_1843_2kbps_1slot	CDMA2000 1xEV-DO Forward	IS-95SPEC+EQ	PN15fix*

Table 3.9-1　List of CDMA2000 1xEV-DO waveform patterns (2/2)

1xEV-DO Waveform Pattern	Supported System	Baseband Filter	Data
FWD_1228_8kbps_2slot	CDMA2000 1xEV-DO Forward	IS-95SPEC+EQ	PN15fix*
FWD_2457_6kbps_1slot	CDMA2000 1xEV-DO Forward	IS-95SPEC+EQ	PN15fix*
FWD_Idle	CDMA2000 1xEV-DO Forward	IS-95SPEC+EQ	–
RVS_9_6kbps_RX	CDMA2000 1xEV-DO Reverse	IS-95SPEC	PN9fix*
RVS_19_2kbps_RX	CDMA2000 1xEV-DO Reverse	IS-95SPEC	PN9fix*
RVS_38_4kbps_RX	CDMA2000 1xEV-DO Reverse	IS-95SPEC	PN9fix*
RVS_76_8kbps_RX	CDMA2000 1xEV-DO Reverse	IS-95SPEC	PN9fix*
RVS_153_6kbps_RX	CDMA2000 1xEV-DO Reverse	IS-95SPEC	PN9fix*
RVS_9_6kbps_TX	CDMA2000 1xEV-DO Reverse	IS-95SPEC	PN9fix*
RVS_19_2kbps_TX	CDMA2000 1xEV-DO Reverse	IS-95SPEC	PN9fix*
RVS_38_4kbps_TX	CDMA2000 1xEV-DO Reverse	IS-95SPEC	PN9fix*
RVS_76_8kbps_TX	CDMA2000 1xEV-DO Reverse	IS-95SPEC	PN9fix*
RVS_153_6kbps_TX	CDMA2000 1xEV-DO Reverse	IS-95SPEC	PN9fix*

*: Indicates the PN sequence that was extracted for each packet. Therefore, the PN sequence is not continuous between the last data of a packet and the first data of the next packet.

When outputting each CDMA2000 1xEV-DO waveform pattern, marker signal (Marker 1, Marker 2, Marker 3) as outlined in the Table 3.9-2 is output from Marker1 Output connector of MG3710A rear panel or from AUX connector. For details of output connector setting, refer to 7.4.2 “Route Output Connectors” in MG3710A Vector Signal Generator Operation Manual (Mainframe).

Table 3.9-2 Marker output data and IQ output level

Marker Signal	Output Data
Marker 1	Frame Clock
Marker 2	RF Gate
Marker 3	Symbol Clock
AWGN addition (Note)	Enable

3.9.1 1xEV-DO forward (excluding FWD_Idle)

When a waveform pattern from FWD_38_4kbps_16slot to FWD_245_7kbps_6_1slot is selected, a CDMA2000 1xEV-DO forward modulated signal for which channel coding and IQ mapping are executed according to 3GPP2 C.S0024 is output. In this output signal, the pilot channel, forward MAC channel, and forward traffic channel are multiplexed. For the forward traffic channel, PN15fix* is used as the data before adding FCS (Frame Check Sequence).
Fig 3.9.1-1 shows the format of PN15fix bit sequence with FCS and TAIL bit sequences added. Hereafter, the PN15fix bit sequence with FCS and TAIL bit sequences added is referred to as “packet”.

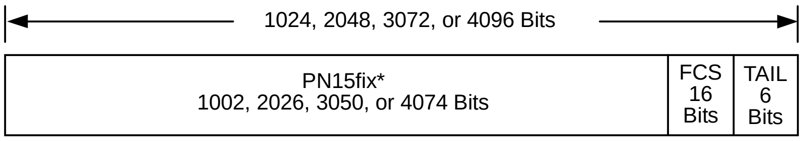


Figure 3.9.1-1 Format of 1xEV-DO forward packet

The channel coding including turbo coding, scrambling, channel interleaving, and modulation (QPSK, 8-PSK, 16QAM) is processed for a packet as shown in Figure 3.9.1-2 Then the packet is multiplexed with other channels by time division (time division multiplexing: TDM) For the MAC index that is used in scrambling, the MAC index value used by the preamble in the same slot is used.

*: Indicates the PN sequence that was extracted for each packet. Therefore, the PN sequence is not continuous between the last data of a packet and the first data of the next packet.

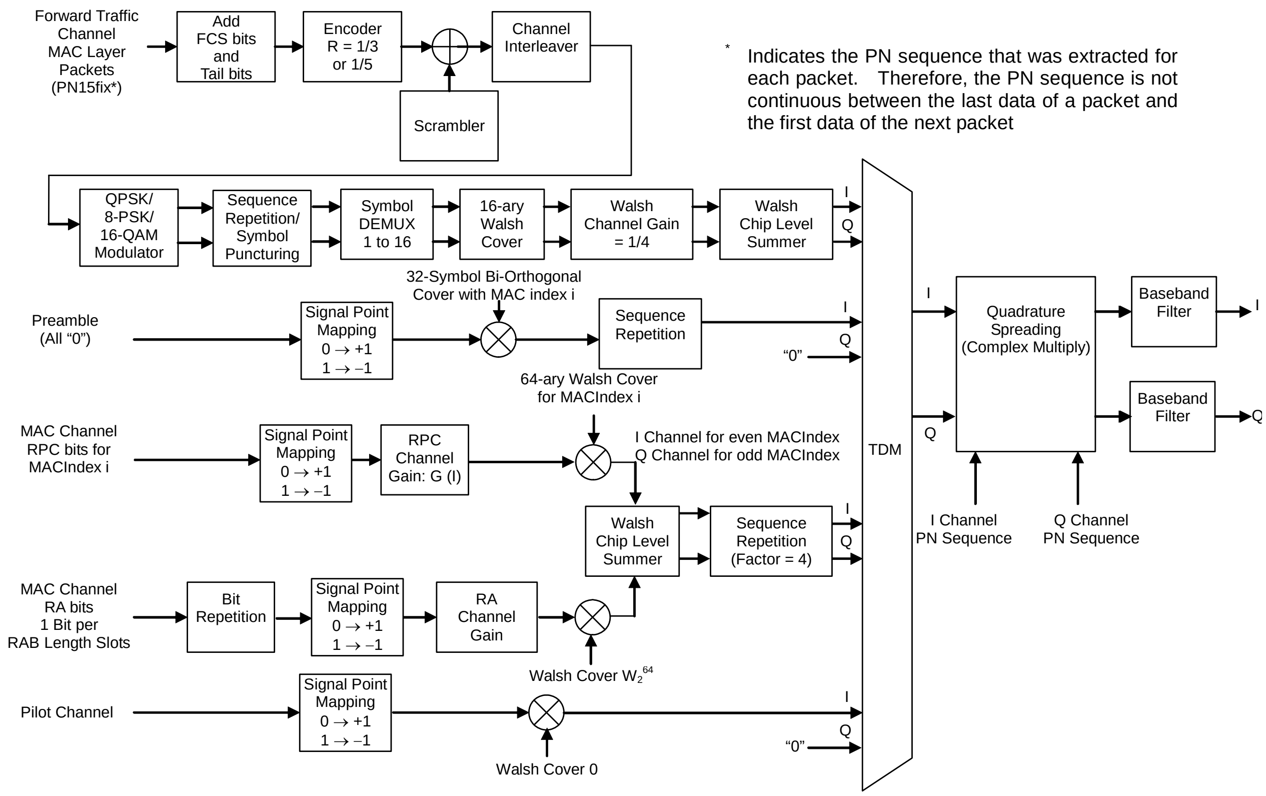


Figure 3.9.1-2 Signal generation block diagram of 1xEV-DO forward waveform pattern

The channel-coded packet is allocated to the data field in the slot along with the preamble that has the same MAC index by time division multiplexing.

Figure 3.9.1-3 shows the slot format, and Fig 3.9.1-4 shows the timing of time division multiplexing of preamble, channel-coded packet, MAC channel, and pilot channel.

Data	MAC	Pilot	MAC	Data	MAC	Pilot	MAC	Data
400 chips	64 chips	96 chips	64 chips	800 chips	64 chips	96 chips	64 chips	400 chips

1 slot = 1.67 ms

Figure 3.9.1-3 Slot format of 1xEV-DO forward waveform pattern (excluding idle slot)

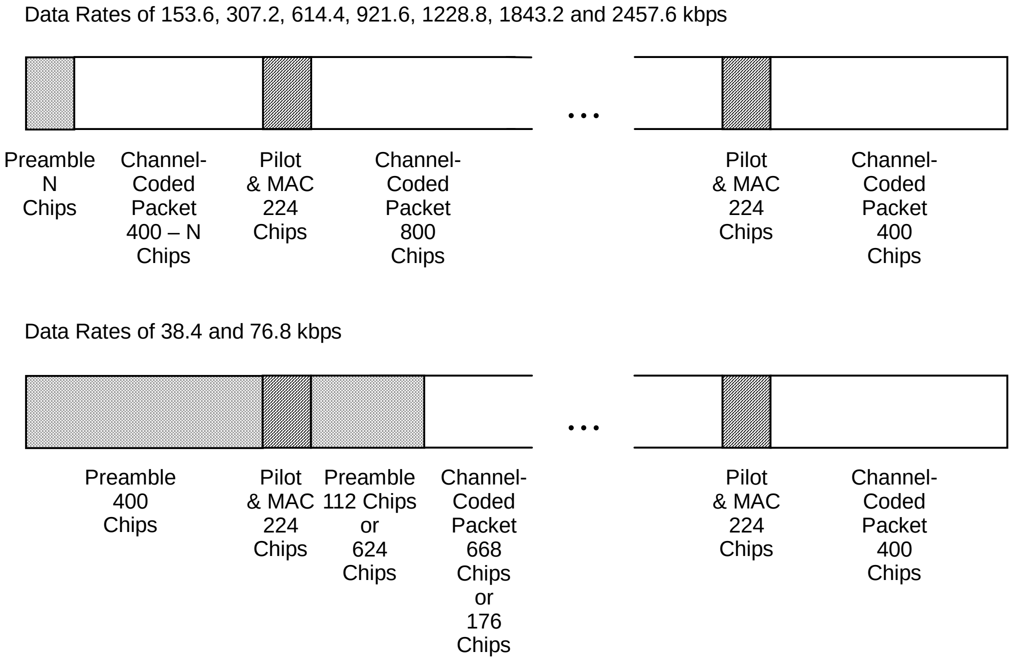


Figure 3.9.1-4 TDM timing diagram

Four PN15fix that have a different initial value of the PN15 code generator are generated as the data to be transferred on the forward traffic channel, and a packet is generated from each PN15fix (four packets in total). Then the channel coding is executed for these packets. At this time, different values are applied to each MAC index that is used by the scrambler, according to each packet. The same MAC index value is applied to the packet and preamble if they are allocated to the same slot. See Figure 3.9.1-5 for MAC index values. A channel-coded packet is allocated to every 4 slots, and another channel-coded packet is allocated to one of the remaining three slots.

Figure 3.9.1-5 shows an example of allocation of forward traffic channels every 4 slots. Table 3.9.1-1 lists the parameters for forward traffic channels.

Table 3.9.1-1 List of traffic channel parameters

1xEV-DO Modulated Signal	Data Rate (kbps)	Slot	Packet (Bit)	Preamble (Chip)	Modulation Type
FWD_38_4kbps_16slot	38.4	16	1024	1024	QPSK
FWD_76_8kbps_8slot	76.8	8	1024	512	QPSK
FWD_153_6kbps_4slot	153.6	4	1024	256	QPSK
FWD_307_2kbps_2slot	307.2	2	1024	128	QPSK
FWD_614_4kbps_1slot	614.4	1	1024	64	QPSK
FWD_307_2kbps_4slot	307.2	4	2048	128	QPSK
FWD_614_4kbps_2slot	614.4	2	2048	64	QPSK
FWD_1228_8kbps_1slot	1228.8	1	2048	64	QPSK
FWD_921_6kbps_2slot	921.6	2	3072	64	8-PSK
FWD_1843_2kbps_1slot	1843.2	1	3072	64	8-PSK
FWD_1228_8kbps_2slot	1228.8	2	4096	64	16QAM
FWD_2457_6kbps_1slot	2457.6	1	4096	64	16QAM

Table 3.9.1-2 lists the parameter for the MAC channel:

Table 3.9.1-2 List of MAC channel parameter

MAC Index	RABit	RPCBit
4 (RA Channel), 5-17 (RPC Channel)	Random	Random

The RPCBit to be transferred on the RPC channel and the RABit to be transferred on the RA channel of the MAC channel are set at random. There are 13 RPC channels and one RA channel. These MAC channels are spread by the Walsh cover, which is determined depending on the MAC index, and then multiplexed. The MAC channels are allocated to the MAC field in a slot as shown in Figure 3.9.1-3. Figure 3.9.1-5 shows the relationship between the slot and the data transmitted by the MAC channel and traffic channel.

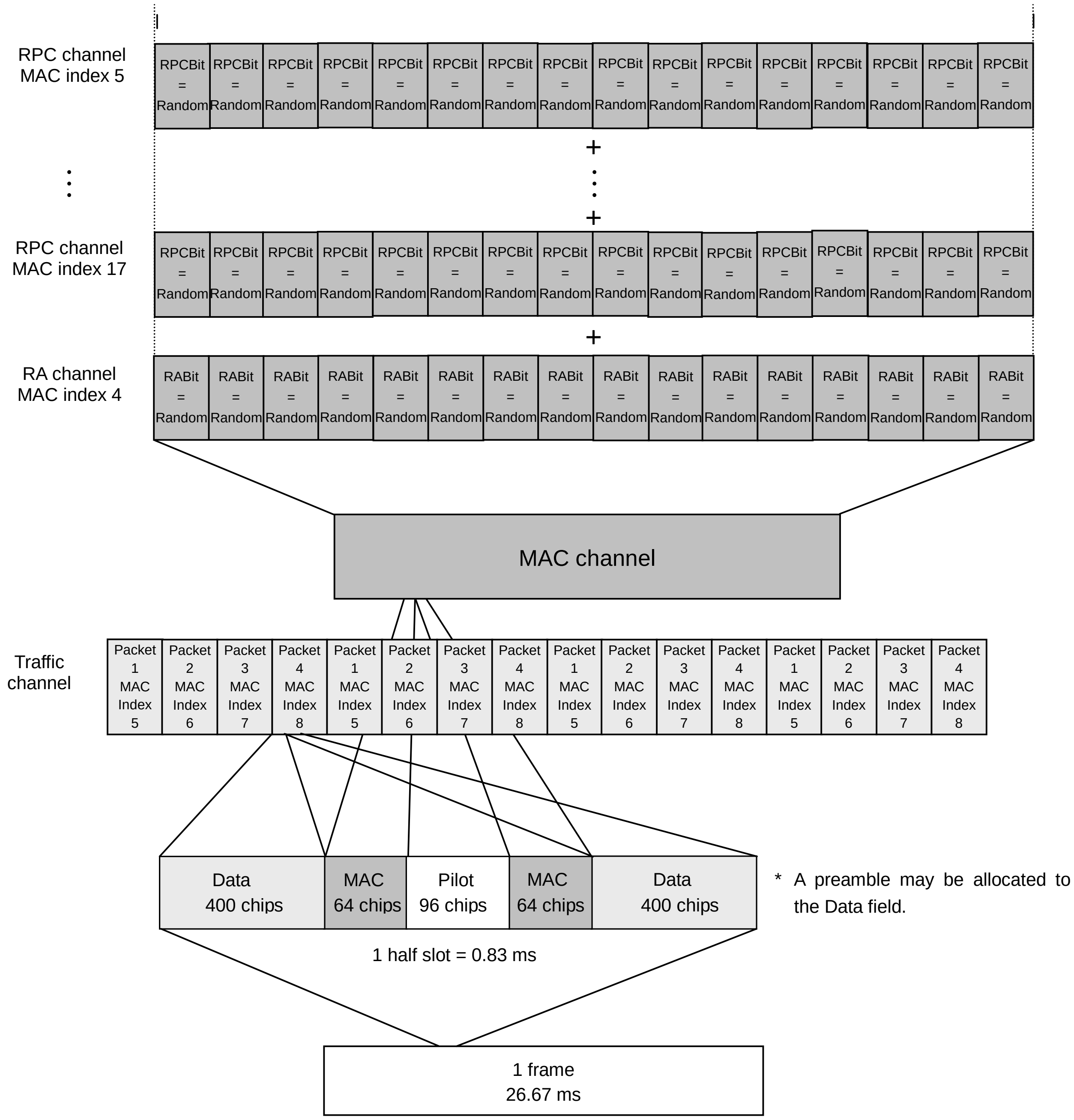


Figure 3.9.1-5 Multiplexing channels

3.9.2 1xEV-DO reverse

When a 1xEV-DO modulated signal from RVS_9_6kbps_RX to RVS_153_6kbps_TX is selected, a CDMA2000 1xEV-DO reverse modulated signal for which channel coding and IQ mapping are executed according to 3GPP2 C.S0024 is output. In this output signal, the pilot channel, RRI channel, DRC channel, ACK channel, and data channel are multiplexed. For the data channel, PN9fix* is used as the data before adding FCS (Frame Check Sequence).
Fig 3.9.2-1 shows the format of PN9fix bit sequence with FCS and TAIL bit sequences added.

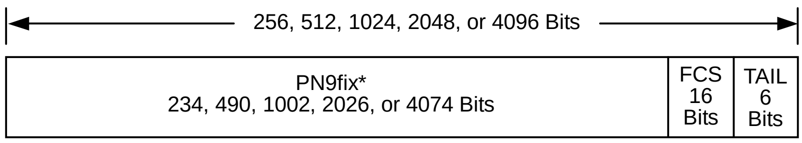
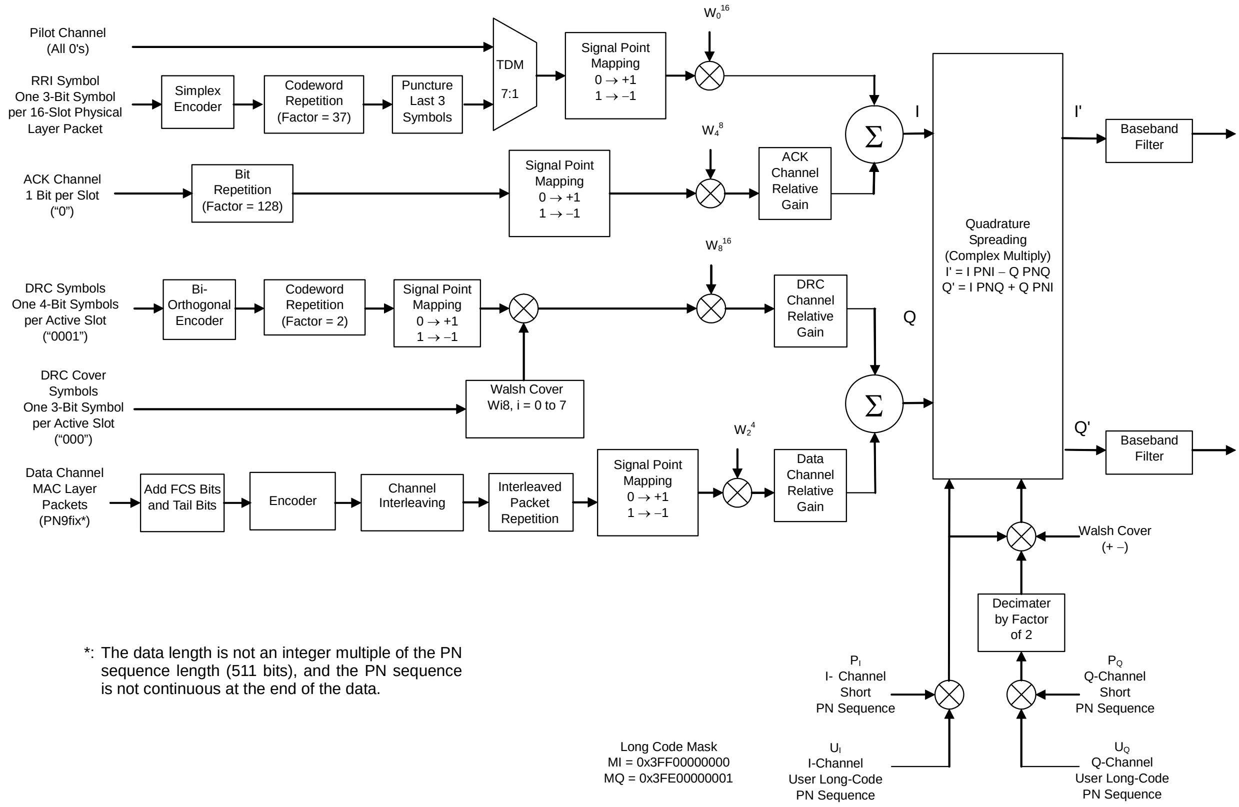


Figure 3.9.2-1 Format of 1xEV-DO reverse packet

The PN9fix bit sequence with FCS and TAIL bit sequences added is channel coded, and then multiplexed with the pilot channel, RRI channel, DRC channel, and ACK channel. Figure 3.9.2-2 shows the block diagram of 1xEV-DO reverse, and Tables 3.9.2-1 and 3.9.2-2 list modulation parameters and channel gains, respectively.

*: The data length is not an integer multiple of the PN sequence length (511 bits), and the PN sequence is not continuous at the end of the data.



*: The data length is not an integer multiple of the PN sequence length (511 bits), and the PN sequence is not continuous at the end of the data.

Figure 3.9.2-2 Signal generation block diagram of 1xEV-DO reverse waveform pattern

Table 3.9.2-1 List of modulation parameters for 1xEV-DO reverse waveform pattern

1xEV-DO Modulated Signal	Data Rate (kbps)	RRI Symbol	DRC Value	DRC Cover	ACK Channel Bit	Long Code Mask
RVS_9_6kbps_RX	9.6	001	0x01	W_0^8	0	MI = 0x3FF00000000 MQ = 0x3FE00000001
RVS_19_2kbps_RX	19.2	010	0x01	W_0^8	0	
RVS_38_4kbps_RX	38.4	011	0x01	W_0^8	0	
RVS_76_8kbps_RX	76.8	100	0x01	W_0^8	0	
RVS_153_6kbps_RX	153.6	101	0x01	W_0^8	0	
RVS_9_6kbps_TX	9.6	001	0x01	W_0^8	0	
RVS_19_2kbps_TX	19.2	010	0x01	W_0^8	0	
RVS_38_4kbps_TX	38.4	011	0x01	W_0^8	0	
RVS_76_8kbps_TX	76.8	100	0x01	W_0^8	0	
RVS_153_6kbps_TX	153.6	101	0x01	W_0^8	0	

Table 3.9.2-2 List of channel gains for 1xEV-DO reverse waveform pattern

1xEV-DO Modulated Signal	Data Rate (kbps)	Data/Pilot	RRI/Pilot	DRC/Pilot	ACK/Pilot
RVS_9_6kbps_RX	9.6	3.75 dB	0 dB	3.0 dB	0.0 dB
RVS_19_2kbps_RX	19.2	6.75 dB	0 dB	3.0 dB	0.0 dB
RVS_38_4kbps_RX	38.4	9.75 dB	0 dB	3.0 dB	0.0 dB
RVS_76_8kbps_RX	76.8	13.25 dB	0 dB	3.0 dB	0.0 dB
RVS_153_6kbps_RX	153.6	18.50 dB	0 dB	3.0 dB	0.0 dB
RVS_9.6 kbps_TX	9.6	3.75 dB	0 dB	3.0 dB	3.0 dB
RVS_19.2 kbps_TX	19.2	6.75 dB	0 dB	3.0 dB	3.0 dB
RVS_38.4 kbps_TX	38.4	9.75 dB	0 dB	3.0 dB	3.0 dB
RVS_76.8 kbps_TX	76.8	13.25 dB	0 dB	3.0 dB	3.0 dB
RVS_153.6 kbps_TX	153.6	18.50 dB	0 dB	3.0 dB	3.0 dB

3.9.3 1xEV-DO forward idle slot

When the FWD_Idle waveform pattern is selected, a modulated signal with the CDMA2000 1xEV-DO forward idle slot configuration for which channel coding and IQ mapping are executed according to 3GPP2 C.S0024 is output. In this output signal, the pilot channel and forward MAC channel are multiplexed. Figure 3.9.3-1 shows the block diagram of 1xEV-DO forward idle slot waveform pattern.

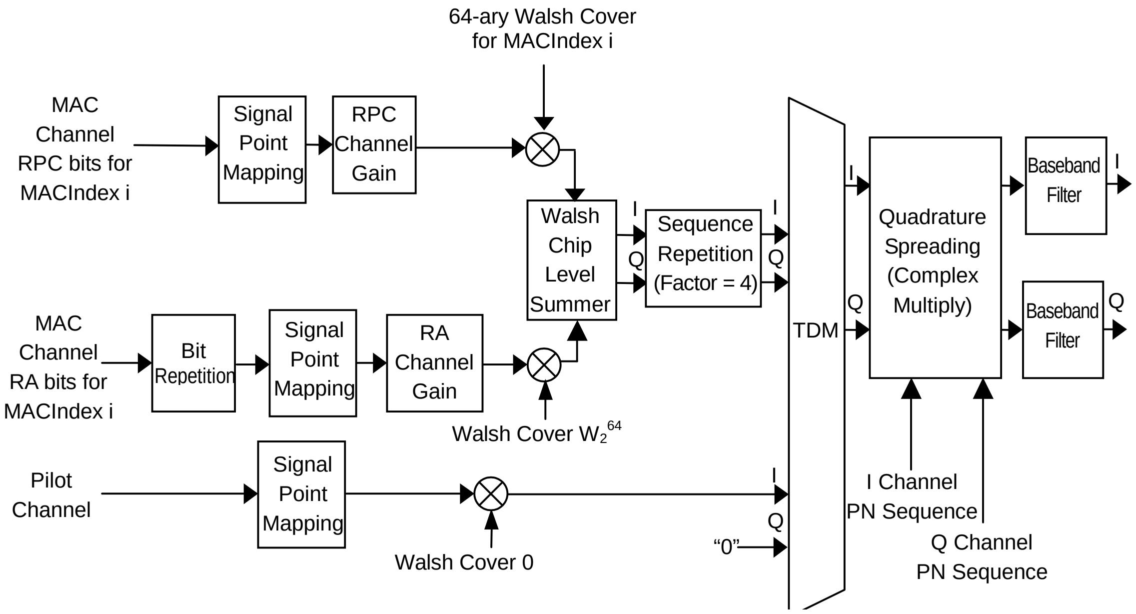


Figure 3.9.3-1 Signal generation block diagram of 1xEV-DO forward idle slot waveform pattern

Figure 3.9.3-2 shows the 1xEV-DO forward idle slot waveform pattern format, and Table 3.9.3-1 lists the MAC channel parameters for the 1xEV-DO forward idle slot waveform pattern.

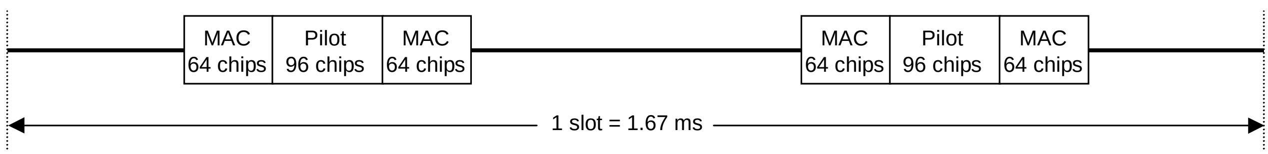


Figure 3.9.3-2 Format of 1xEV-DO forward idle slot waveform pattern

Table 3.9.3-1 List of MAC channel parameters for 1xEV-DO forward idle slot waveform pattern

MAC Index	RA Bit	RPC Bit	RA Channel Gain	RPC Channel Gain
4 (RA Channel), 5 to 17 (RPC Channel)	Random	Random	–12.04 dB*	–11.42 dB*

*: Relative value to the pilot channel.

3.10 WLAN Waveform Pattern

As the WLAN waveform pattern, waveform patterns that conform to IEEE802.11a/b/g are provided as shown.

Table 3.10-1 List of IEEE802.11a waveform patterns

Waveform Pattern Name	Data Rate (Mbits/s)	Modulation	Coding Rate	Coding Bits per Subcarrier	Coding Bits per OFDM Symbol	Data Bits per OFDM Symbol
Package name: WLAN						
11a_OFDM_6Mbps	6	BPSK	1/2	1	48	24
11a_OFDM_9Mbps	9	BPSK	3/4	1	48	36
11a_OFDM_9Mbps_PN9 *1	9	BPSK	3/4	1	48	36
11a_OFDM_12Mbps	12	QPSK	1/2	2	96	48
11a_OFDM_18Mbps	18	QPSK	3/4	2	96	72
11a_OFDM_18Mbps_PN9*1	18	QPSK	3/4	2	96	72
11a_OFDM_24Mbps	24	16-QAM	1/2	4	192	96
11a_OFDM_36Mbps	36	16-QAM	3/4	4	192	144
11a_OFDM_36Mbps_PN9 *1	36	16-QAM	3/4	4	192	144
11a_OFDM_48Mbps	48	64-QAM	2/3	6	288	192
11a_OFDM_54Mbps	54	64-QAM	3/4	6	288	216
11a_OFDM_54Mbps_PN9 *1	54	64-QAM	3/4	6	288	216
11a_OFDM_54Mbps_ACP *2	54	64-QAM	3/4	6	288	216

*1: Waveform pattern having continuous PN9 data. For the waveform patterns without *1 affixed, the PN9 data does not have continuity. A gap period of 4 samples is secured at the start of the waveform pattern, followed by a PLCP preamble. When using an external trigger, set the trigger delay to –4 samples to match the rising of the external trigger and the starting point of the PLCP preamble.

*2: Waveform pattern having improved ACPR with spectrum sidelobes cut down.

Table 3.10-2 List of IEEE802.11b waveform patterns

Waveform Pattern Name	Spreading, Coding	Modulation
Package name: WLAN		
11b_DSSS_1Mbps	DSSS, 11 chip Barker Code	DBPSK
11b_DSSS_2Mbps	DSSS, 11 chip Barker Code	DQPSK
11b_DSSS_2Mbps_PN9*1, *2	DSSS, 11 chip Barker Code	DQPSK
11b_CCK_5_5Mbps	CCK	DQPSK
11b_CCK_11Mbps	CCK	DQPSK
11b_CCK_11Mbps_PN9*1	CCK	DQPSK
11b_CCK_11Mbps_ACP*3	CCK	DQPSK

In the above waveform patterns, the ramp rises at the start of the waveform pattern. The frame clock also rises at the same timing. When using an external trigger, set the trigger delay to −88 samples to match the rising of the external trigger and the starting point of the PLCP preamble.

*1: Waveform pattern having continuous PN9 data. For the waveform patterns without *1 affixed, the PN9 data does not have continuity.

*2: To use this waveform pattern, Combination of Baseband Signal (option), ARB Memory Upgrade 256 Msample (option), or ARB Memory Upgrade 1024 Msample (option), is required.

*3: Waveform pattern having improved ACPR with spectrum sidelobes cut down.

Table 3.10-3 List of IEEE802.11g waveform patterns

Waveform Pattern Name	Data rate (Mbits/s)	Modulation	Coding Rate	Coding Bits per Subcarrier	Coding Bits per OFDM Symbol	Data Bits per OFDM Symbol
Package name: WLAN						
11g_DSSS_OFDM_6Mbps	6	BPSK	1/2	1	48	24
11g_DSSS_OFDM_9Mbps	9	BPSK	3/4	1	48	36
11g_DSSS_OFDM_12Mbps	12	QPSK	1/2	2	96	48
11g_DSSS_OFDM_18Mbps	18	QPSK	3/4	2	96	72
11g_DSSS_OFDM_24Mbps	24	16-QAM	1/2	4	192	96
11g_DSSS_OFDM_36Mbps	36	16-QAM	3/4	4	192	144
11g_DSSS_OFDM_48Mbps	48	64-QAM	2/3	6	288	192
11g_DSSS_OFDM_54Mbps	54	64-QAM	3/4	6	288	216

In the above waveform patterns, the ramp rises at the start of the waveform pattern. The frame clock also rises at the same timing. When using an external trigger, set the trigger delay to –60 samples to match the rising of the external trigger and the starting point of the PLCP preamble.

When outputting each WLAN waveform pattern, marker signal (Marker 1, Marker 2) as outlined in the Table 3.10-4 is output from Marker1 Output connector of MG3710A rear panel or from AUX connector. For details of output connector setting, refer to 7.4.2 "Route Output Connectors" in MG3710A Vector Signal Generator Operation Manual (Mainframe).

Table 3.10-4 Marker output data and IQ output level

Marker Signal	Output Data
Marker 1	Frame Clock
Marker 2	RF Gate
Marker 3	–

3.10.1 IEEE802.11a

These waveform patterns conform to the MAC layer and physical layer standards described in IEEE802.11, IEEE802.11a.

Table 3.10.1-1 lists the parameters commonly used by each waveform pattern:

Table 3.10.1-1 List of common parameters

Parameter	Setting Value
PSDU Length	1000 bytes
PSDU Data	PN9fix or PN9 (Note)
Sampling rate	40 MHz

Note:

PN9fix is PN9 data reset for each PSDU. Therefore, the PN data is not continuous between PSDUs. However, the waveform patterns whose name has _PN9 have the continued PN9 data.

Figure 3.10.1-1 shows the PPDU frame format.

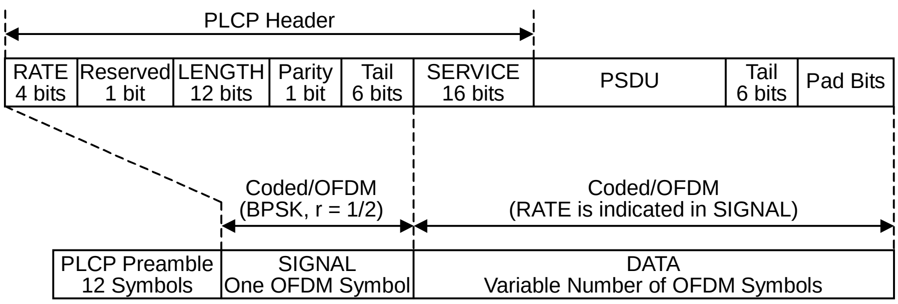


Figure 3.10.1-1 IEEE802.11a PPDU frame format

A MAC frame shown in Figure 3.10.1-2 below is applied to the PSDU field in the PPDU frame format. A MAC frame consists of the MAC header field and FSC field, as well as the transmission data indicated by Frame Body.

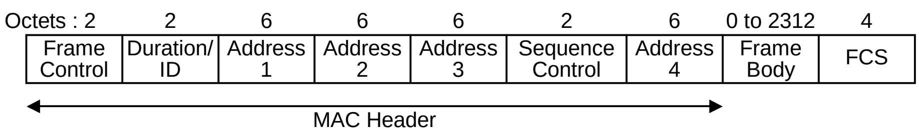


Figure 3.10.1-2 IEEE802.11a MAC frame format

The Frame Control field consists of the following bits with the corresponding data as shown in Table 3.10.1-2 below.

Table 3.10.1-2 Contents of Frame Control field

Field	Bit	Data
Protocol Version	B0 and B1	00
Type	B2 and B3	01
Subtype	B4 to B7	0000
To DS	B8	0
From DS	B9	0
More Flag	B10	0
Retry	B11	0
Power Management	B12	00
More Data	B13	0
WEP	B14	0
Order	B15	0

Table 3.10.1-3 lists the data in a MAC header excluding the Frame Control field.

Table 3.10.1-3 Contents of MAC header excluding Frame Control field

Field	Data
Duration/ID	0000_H
Address 1	FFFF FFFF $FFFF_H$ (Note)
Address 2	0000 0000 0000_H
Address 3	0000 0000 0000_H
Sequence Control	0000_H
Address 4	0000 0000 0000_H

Note:

For Address 1 (Destination Address in the Adhoc mode,) all “1” indicates broadcast address.

3.10.2 IEEE802.11b

These waveform patterns conform to the MAC layer and physical layer standards described in IEEE802.11, IEEE802.11b.

Table 3.10.2-1 lists the parameters commonly used by each waveform pattern:

Table 3.10.2-1 List of common parameters

Parameter	Setting Value
PSDU Length	1024 bytes
PSDU Data	PN9fix or PN9 (Note)
Sampling rate	44 MHz

Note:

PN9fix is PN9 data reset for each PSDU. Therefore, the PN data is not continuous between PSDUs. However, the waveform patterns whose name has _PN9 have the continued PN9 data.

Figure 3.10.2-1 shows the Long PLCP PPDU frame format.

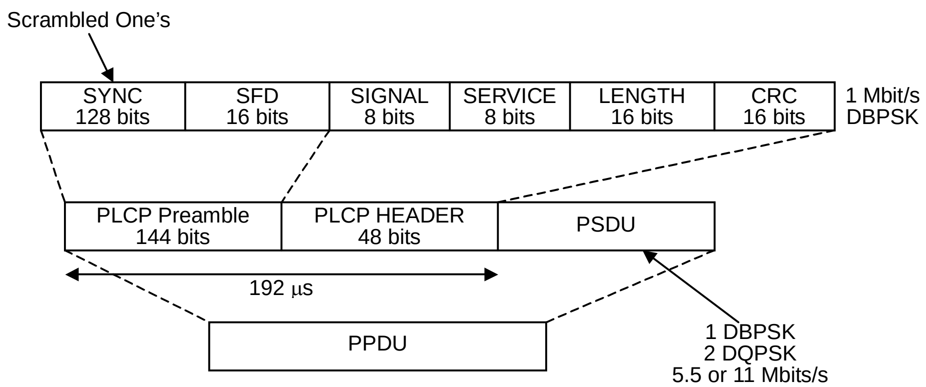


Figure 3.10.2-1 IEEE802.11b Long PLCP PPDU frame format

A MAC frame same with that described in Section 3.8.1 "IEEE802.11a" is applied to the PSDU field in the Long PLCP PPDU frame format.

3.10.3 IEEE802.11g

These waveform patterns conform to the physical layer standards described in IEEE802.11, IEEE802.11g.

Table 3.10.3-1 lists the parameters commonly used by each waveform pattern:

Table 3.10.3-1   List of common parameters

Parameter	Setting Value
PSDU Length	1000 bytes
PSDU Data	PN9fix (Note)
Sampling rate	44 MHz

Note:

PN9fix is PN9 data reset for each PSDU. Therefore, the PN data is not continuous between PSDUs.

Figure 3.10.3-1 shows the Long PLCP PPDU frame format.

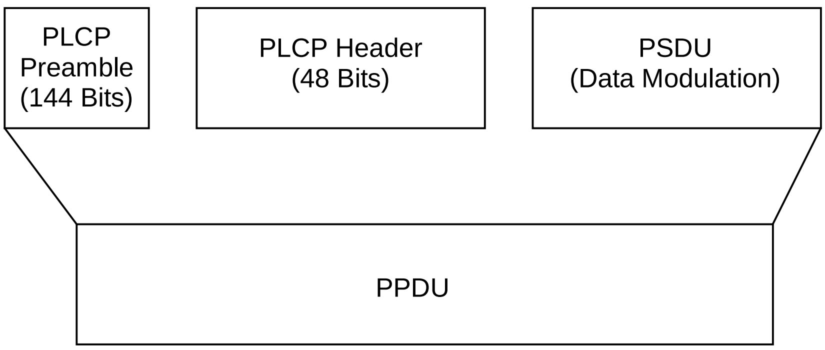


Figure 3.10.3-1   IEEE802.11b Long preamble PPDU frame format

3.11 Digital Broadcast Waveform Pattern

The Digital Broadcast waveform patterns shown in Table 3.11-1 are provided.

Table 3.11-1 List of Digital Broadcast waveform patterns

Waveform Pattern Name	Parameter	Application
Package name: Digital_Broadcast		
BS_1ch	Roll-off factor: 0.35 Nyquist Bandwidth: 28.86 MHz Modulation: QPSK	Physical layer waveform pattern of digital BS broadcast for device evaluation.
CS_1ch	Roll-off factor: 0.35 Nyquist Bandwidth: 21.096 MHz Modulation: QPSK	Physical layer waveform pattern of digital CS broadcast for device evaluation.
CATV_AnnexC_1ch	Roll-off factor: 0.13 Nyquist Bandwidth: 5.274 MHz Modulation: 64QAM	Physical layer waveform pattern of CATV (ITU-T J83 Annex C) for device evaluation.
ISDBT_1layer_1ch	Mode: 3, GI: 1/8 A-Layer:13seg, 64QAM	Physical layer waveform pattern of ISDB-T for device evaluation.
ISDBT_2layer_1ch	Mode: 3, GI: 1/8 A-Layer: 1seg, QPSK B-Layer: 12seg, 64QAM	Physical layer waveform pattern of ISDB-T for device evaluation.
ISDBT_2layer_Movie *1	Mode: 3, GI: 1/8 A-Layer: 1seg, QPSK, CR = 2/3, TI = 2 B-Layer: 12seg, 64QAM, CR = 7/8, TI = 2	Waveform pattern for ISDB-T partial reception, mainly used for evaluation of image and voice data of terminals. The waveform length is 40 frames. *2
ISDBT_2layer_Movie2 *1	Mode: 3, GI: 1/8 A-Layer: 1seg, QPSK, CR = 2/3, TI = 4 B-Layer: 12seg, 64QAM, CR = 3/4, TI = 2	
ISDBT_2layer_Coded	Mode: 3, GI: 1/8 A-Layer: 1seg, QPSK, CR = 2/3, TI = 2 B-Layer: 12seg, 64QAM, CR = 7/8, TI = 2	Waveform pattern for ISDB-T partial reception, mainly used for simple BER measurement. The waveform length is 4 frames.
ISDBT_QPSK_1_2	Mode: 3, GI: 1/8 A-Layer: 1seg, QPSK, CR = 1/2, TI = 0 B-Layer: 12seg, 64QAM, CR = 7/8, TI = 1	Waveform pattern for ISDB-T partial reception, mainly used for simple BER measurement. The waveform length is 4 frames.
ISDBT_QPSK_2_3	Mode: 3, GI: 1/8 A-Layer: 1seg, QPSK, CR = 2/3, TI = 0 B-Layer: 12seg, 64QAM, CR = 7/8, TI =1	
ISDBT_16QAM_1_2	Mode: 3, GI: 1/8 A-Layer: 1seg, 16QAM, CR = 1/2, TI = 0 B-Layer: 12seg, 64QAM, CR = 7/8, TI = 1	

Table 3.11-1 List of Digital Broadcast waveform patterns (Cont'd)

Waveform Pattern Name	Parameter	Application
ISDBT_QPSK_2_3_TI4	Mode: 3, GI: 1/8 A-Layer: 1seg, QPSK, CR = 2/3, TI = 4 B-Layer: 12seg, 64QAM, CR = 3/4, TI = 2	
ISDBTsb_Movie *3	Seg#1 to #5: 8-segment concatenation transmission in 1-segment format Seg#6 to #8: 8-segment concatenation transmission in 3-segment format Mode: 3, GI: 1/8 A-Layer: QPSK, CR = 1/2, TI = 4 B-Layer: QPSK, CR = 1/2, TI = 4	Mainly used for evaluation of image and voice data of terminals. The waveform length is 68 frames.*2
ISDBTsb_QPSK_1_2	Seg#1 to #5: 8-segment concatenation transmission in 1-segment format Seg#6 to #8: 8-segment concatenation transmission in 3-segment format Mode: 3, GI: 1/8 A-Layer: QPSK, CR = 1/2, TI = 0 B-Layer: QPSK, CR = 1/2, TI = 0	Mainly used for simple BER measurement. The waveform length is 4 frames.
ISDBTsb_QPSK_2_3	Seg#1 to #5: 8-segment concatenation transmission in 1-segment format Seg#6 to #8: 8-segment concatenation transmission in 3-segment format Mode: 3, GI: 1/8 A-Layer: QPSK, CR = 2/3, TI = 0 B-Layer: QPSK, CR = 2/3, TI = 0	
ISDBTsb_16QAM_1_2	Seg#1 to #5: 8-segment concatenation transmission in 1-segment format Seg#6 to #8: 8-segment concatenation transmission in 3-segment format Mode: 3, GI: 1/8 A-Layer: 16QAM, CR = 1/2, TI = 0 B-Layer: 16QAM, CR = 1/2, TI = 0	

*1: To use this waveform pattern, ARB Memory Upgrade 256 Msample (option) or ARB Memory Upgrade 1024 Msample (option), is required.

*2: It is not guaranteed that any receiver can receive a waveform with this length.

*3: To use this waveform pattern, Combination of Baseband Signal (option), ARB Memory Upgrade 256 Msample (option), or ARB Memory Upgrade 1024 Msample (option), is required.

Table 3.11-2 lists the parameters commonly used by each waveform pattern.

Table 3.11-2 List of common parameters

Parameter	Setting Value
Data	PN23fix*: (digital BS, digital CS, CATV, ISDB-T)
Sampling rate	digital BS: 144.3 Msps digital CS: 147.62 Msps CATV: 42.192 Msps ISDB-T: 16.253968 Msps ISDB-Tsb: 8.12698417 Msps

*: PN sequence is discontinuous at the connection of the waveform pattern.

3.11.1 Frame configuration

BS_1ch, CS_1ch, CATV_AnnexC_1ch

Digital BS, digital CS and CATV waveform patterns have no-frame structure as follows.

Figure 3.11.1-1 Data structure for digital BS, digital CS and CATV

ISDBT_1layer_1ch, ISDBT_2layer_1ch, ISDBT_QPSK_1_2, ISDBT_QPSK_2_3, ISDBT_16QAM_1_2, ISDBT_QPSK_2_3_TI4

ISDB-T waveform patterns are created as follows.

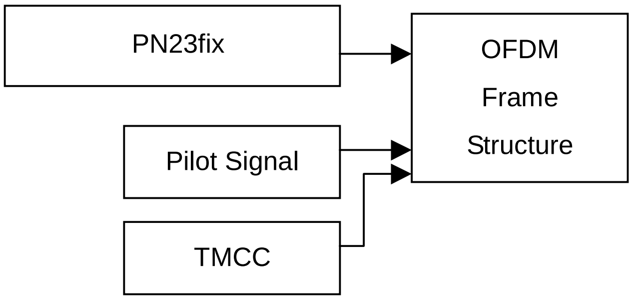


Figure 3.11.1-2 Generation of the waveform patterns for ISDB-T

ISDBT_2layer_Movie, ISDBT_2layer_Movie2, ISDBT_2layer_Coded

ISDB-T waveform patterns are created as follows.

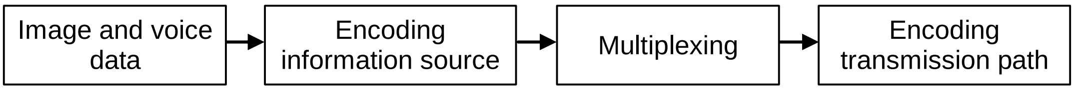


Figure 3.11.1-3 Generation of the waveform patterns for ISDB-T

Table 3.11.1-1 lists the parameters used for encoding the transmission paths of ISDBT_2layer_Movie and ISDBT_2layer_Coded waveform patterns.

Table 3.11.1-2 lists the parameters used for encoding the transmission paths of an ISDBT_2layer_Movie2 waveform pattern.

Image and voice data of receivers for partial reception can be evaluated with ISDBT_2layer_Movie and ISDBT_2layer_Movie2 waveform patterns.

Simple BER measurement can be performed for receivers for partial reception with an ISDBT_2layer_Coded waveform pattern.
Note that the contents in Layers A and B of ISDBT_2layer_Movie waveform patterns, those of ISDBT_2layer_Movie2 waveform patterns, and those of ISDBT_2layer_Coded waveform patterns are different.

Table 3.11.1-1 List of transmission path encoding parameters for ISDBT_2layer_Movie and ISDBT_2layer_Coded waveform patterns

Parameter	Layer A	Layer B
Mode	Mode3	
Guard interval	1/8	
Partial reception	ON	
Emergency flag	OFF	
Segment count	1	12
Modulation	QPSK	64QAM
Encoding rate	2/3	7/8
Time interleave	2	2

Table 3.11.1-2 List of transmission path encoding parameters for ISDBT_2layer_Movie2 waveform pattern

Parameter	Layer A	Layer B
Mode	Mode3	
Guard interval	1/8	
Partial reception	ON	
Emergency flag	OFF	
Segment count	1	12
Modulation	QPSK	64QAM
Encoding rate	2/3	3/4
Time interleave	4	2

Table 3.11.1-3 lists the parameters used for encoding the transmission paths for each segment of ISDBTsb_Movie waveform patterns. Signals in 1-segment format or signals in 3-segment format are concatenated into 8 segments in a layout shown in Table 3.11.1-3 and transmitted.

Table 3.11.1-3 List of transmission path encoding parameters for ISDBTsb_Movie waveform patterns

Parameter	Seg#1	Seg#2	Seg#3	Seg#4	Seg#5	Seg#6 to #8	
Layer	Layer A	Layer A	Layer A	Layer A	Layer A	Layer A	Layer B
Mode	Mode3						
Guard interval	1/8						
Partial reception	OFF	OFF	OFF	OFF	OFF	ON	OFF
Emergency flag	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Modulation	QPSK	QPSK	QPSK	QPSK	QPSK	QPSK	QPSK
Encoding rate	1/2	1/2	1/2	1/2	1/2	1/2	1/2
Time interleave	4	4	4	4	4	4	4
Subchannel No. in the center of segment	5	8	11	14	17	20/23/26	

An ISDBTsb_Movie waveform pattern contains image and voice data that are multiplexed, re-multiplexed, and encoded. Table 3.11.1-4 lists the multiplexed parameters. Images and voices of the receiver can be evaluated using such a waveform pattern. When receiving an RF signal, set the output frequency of the MG3710A to 190.21428571 MHz.

Table 3.11.1-4 PSI/SI information of ISDBTsb_Movie waveform pattern

Parameter	Seg#1	Seg#2	Seg#3	Seg#4	Seg#5	Seg#6 to 8
service_id	0x2600	0x2608	0x2610	0x2618	0x2620	0x2630
network_id	0x8090	0x8091	0x8092	0x8093	0x8094	0x8096
transport_stream_id	0x8090	0x8091	0x8092	0x8093	0x8094	0x8096
remote_control_key_id	0x5B	0x5C	0x5D	0x5E	0x5F	0x60
frequency	0x529	0x52C	0x52F	0x532	0x535	0x538
connected_transmission_group_id	0x2401	0x2401	0x2401	0x2401	0x2401	0x2401

3.12 Bluetooth® Waveform Pattern

The *Bluetooth* waveform patterns shown in Table 3.12-1 are provided.

Table 3.12-1 List of *Bluetooth* waveform patterns (1/2)

Waveform Pattern Name	Data rate (Mbits/s)	Modulation for Payload	Filter	Packet Type	Dirty, FM*8
Package name: Bluetooth					
DH1*1	1	GFSK*4	Gaussian*5	DH1	-
DH3*1	1	GFSK*4	Gaussian*5	DH3	-
DH5*1	1	GFSK*4	Gaussian*5	DH5	-
DH3_3SlotOff*1	1	GFSK*4	Gaussian*5	DH3	-
DH5_5SlotOff*1	1	GFSK*4	Gaussian*5	DH5	-
POLL	1	GFSK*4	Gaussian*5	POLL	-
2-DH1*1	2	π/4-DQPSK	Root Nyquist*6	2-DH1	-
2-DH3*1	2	π/4-DQPSK	Root Nyquist*6	2-DH3	-
2-DH5*1	2	π/4-DQPSK	Root Nyquist*6	2-DH5	-
2-DH3_3SlotOff*1	2	π/4-DQPSK	Root Nyquist*6	2-DH3	-
2-DH5_5SlotOff*1	2	π/4-DQPSK	Root Nyquist*6	2-DH5	-
3-DH1*1	3	8-DPSK	Root Nyquist*6	3-DH1	-
3-DH3*1	3	8-DPSK	Root Nyquist*6	3-DH3	-
3-DH5*1	3	8-DPSK	Root Nyquist*6	3-DH5	-
3-DH3_3SlotOff*1	3	8-DPSK	Root Nyquist*6	3-DH3	-
3-DH5_5SlotOff*1	3	8-DPSK	Root Nyquist*6	3-DH5	-
GFSK-PN9*2	1	GFSK*4	Gaussian*5	No packet format	-
GFSK-PN15*3	1	GFSK*4	Gaussian*5	No packet format	-
PI_4_DQPSK-PN9*2	2	π/4-DQPSK	Root Nyquist*6	No packet format	-
PI_4_DQPSK-PN15*3	2	π/4-DQPSK	Root Nyquist*6	No packet format	-
8DPSK-PN9*2	3	8DPSK	Root Nyquist*6	No packet format	-
8DPSK-PN15*3	3	8DPSK	Root Nyquist*6	No packet format	-

Table 3.12-1 List of *Bluetooth* waveform patterns (2/2)

Waveform Pattern Name	Data rate (Mbits/s)	Modulation for Payload	Filter	Packet Type	Dirty, FM*8
DH1_dirty*1	1	GFSK*4	Gaussian*5	DH1	Dirty
DH3_dirty *1	1	GFSK*4	Gaussian*5	DH3	Dirty
DH5_dirty *1	1	GFSK*4	Gaussian*5	DH5	Dirty
2-DH1_dirty *1	2	π/4-DQPSK	Root Nyquist*6	2-DH1	Dirty
2-DH3_dirty *1	2	π/4-DQPSK	Root Nyquist*6	2-DH3	Dirty
2-DH5_dirty *1	2	π/4-DQPSK	Root Nyquist*6	2-DH5	Dirty
3-DH1_dirty *1	3	8-DPSK	Root Nyquist*6	3-DH1	Dirty
3-DH3_dirty *1	3	8-DPSK	Root Nyquist*6	3-DH3	Dirty
3-DH5_dirty *1	3	8-DPSK	Root Nyquist*6	3-DH5	Dirty
DH1_Dirty_withFM*1	1	GFSK*4	Gaussian*5	DH1	Dirty, FM
DH3_Dirty_withFM*1	1	GFSK*4	Gaussian*5	DH3	Dirty, FM
DH5_Dirty_withFM*1	1	GFSK*4	Gaussian*5	DH5	Dirty, FM
2-DH1_Dirty_withFM *1	2	π/4-DQPSK	Root Nyquist*6	2-DH1	Dirty, FM
2-DH3_Dirty_withFM *1	2	π/4-DQPSK	Root Nyquist*6	2-DH3	Dirty, FM
2-DH5_Dirty_withFM *1	2	π/4-DQPSK	Root Nyquist*6	2-DH5	Dirty, FM
3-DH1_Dirty_withFM *1	3	8-DPSK	Root Nyquist*6	3-DH1	Dirty, FM
3-DH3_Dirty_withFM *1	3	8-DPSK	Root Nyquist*6	3-DH3	Dirty, FM
3-DH5_Dirty_withFM *1	3	8-DPSK	Root Nyquist*6	3-DH5	Dirty, FM
BLE*1	1	GFSK*9	Gaussian*5	BLE Reference Signal	-
BLE_Dirty*1	1	GFSK*9	Gaussian*5	BLE Reference Signal	Dirty
BLE_Dirty_withFM*1	1	GFSK*9	Gaussian*5	BLE Reference Signal	Dirty, FM
BLE_CRC_corrupted *1,*7	1	GFSK*9	Gaussian*5	BLE Reference Signal	-
GFSK-PN15_BLE*3	1	GFSK*9	Gaussian*5	No packet format	-

*1: PN9 data is inserted into the payload body.

*2: PN9 data is inserted to all areas that do not have a packet format.

*3: PN15 data is inserted to all areas that do not have a packet format.

*4: Modulation index = 0.32

*5: Bandwidth time (BT) = 0.5

*6: Roll-off rate β = 0.4

*7: Use in RF-PHY.TS/4.0.0 RCV-LE/CA/07/C (PER Report Integrity) with intentional CRC errors in every other packet is assumed.

*8: Refer to Section 3.12.4.

*9: Modulation index = 0.5

Figure 3.12-1 below shows the timing chart of waveform patterns that have a packet format.

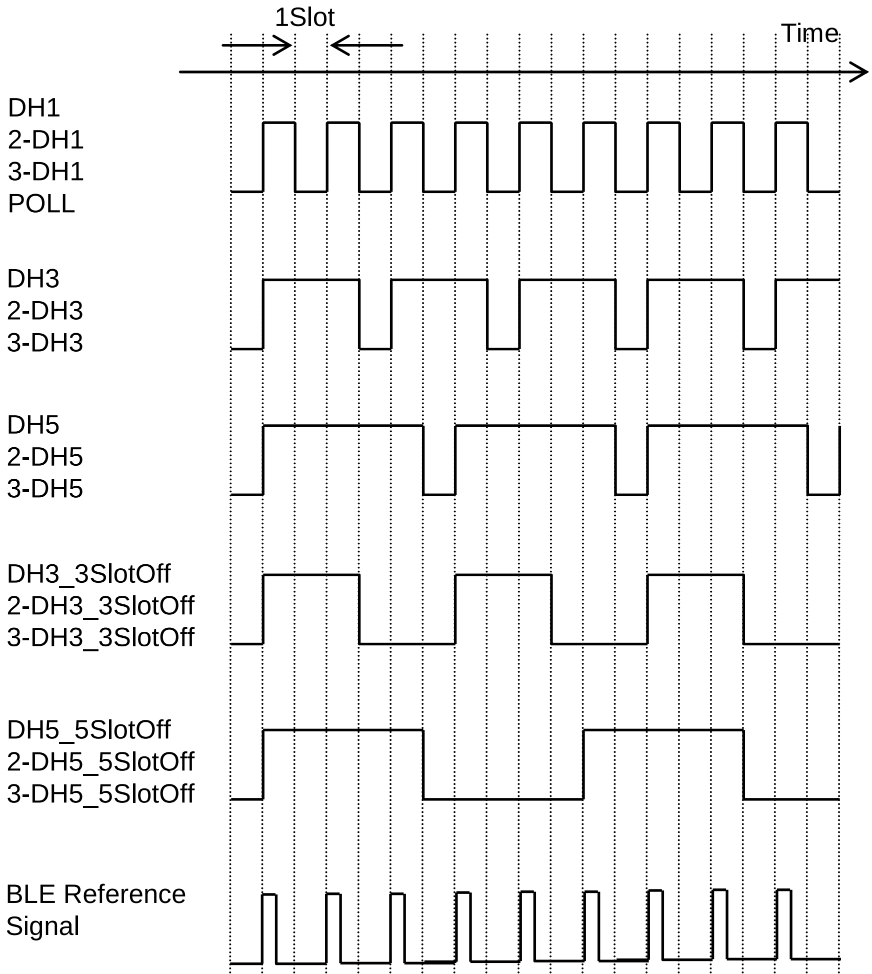


Figure 3.12-1 Timing chart of waveform patterns

When outputting each *Bluetooth* waveform pattern with packet configuration, marker signal (Marker 1, Marker 2) as outlined in the Table 3.12-2 is output from Marker1 Output connector of MG3710A rear panel or from AUX connector. For details of output connector setting, refer to 7.4.2 “Route Output Connectors” in MG3710A Vector Signal Generator Operation Manual (Mainframe).

Table 3.12-2 Marker output data and IQ output level

Marker Signal	Output Data
Marker 1	Packet Clock
Marker 2	RF Gate
Marker 3	–

3.12.1 Packet configuration for Basic Rate (BR)

When a waveform pattern of DH1, DH3, DH5, DH3_3SlotOff, or DH5_5SlotOff is selected, the data is output in the format shown in Figure 3.12.1-1 below. Table 3.12.1-1 shows the payload body data length for each file.

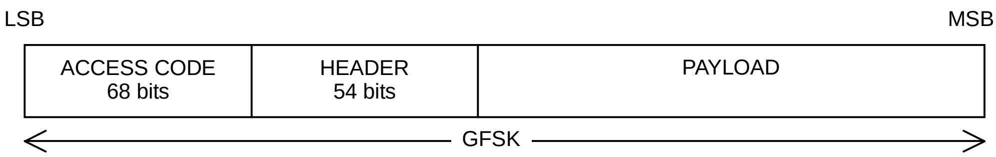


Figure 3.12.1-1 Packet configuration for Basic Rate waveform

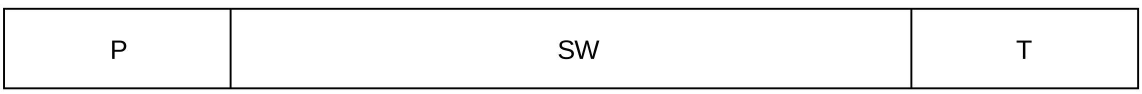
Table 3.12.1-1 Data length of payload body for BR

Packet Type	Payload Body (Bytes)
DH1	27
DH3	183
DH5	339
POLL	None

3.12.1.1 ACCESS CODE

The following figure shows the configuration of the ACCESS CODE. For Sync Word (SW), a value that is obtained according to the Sync Word Definition, which is prescribed in section 6.3.3 of BLUETOOTH SPECIFICATION Version 2.0 + EDR[vol3], is assigned with LAP = $9E8B33_H$. For Preamble and Trailer, a value that is determined by the Sync Word value and the specifications in section 6.3.2 (for Preamble) or 6.3.4 (for Trailer) of the above specifications is assigned respectively.

ACCESS CODE



P:	Preamble	5_H (4 bits)
SW:	Sync Word	$475C58CC73345E72_H$ (64 bits)
T:	Trailer	A_H (4 bits)

3.12.1.2 Packet Header

The following figure shows the configuration of the Packet Header. For HEC, a value that is obtained according to the HEC generation specifications, which are prescribed in section 7.1.1 of BLUETOOTH SPECIFICATION Version 2.0 + EDR[vol3], is assigned. 18-bit HEC data is then converted to 54-bit data, according to FEC: RATE 1/3, which is prescribed in section 7.4 of BLUETOOTH SPECIFICATION Version 2.0 + EDR[vol3].

Packet Header

LT_ADDR	TYPE	FLOW	ARQN	SEQN	HEC

LT_ADDR:	Logical transport address	0_H (3 bits)
FLOW:	Flow control	1_H (1 bit)
ARQN:	Acknowledge indication	1_H (1 bit)
SEQN:	Sequence number	Alternate of 1_H and 0_H (1 bit)
HEC:	Header error check	(18 bits)

Table 3.12.1.2-1 Type code (TYPE) for BR output signal

Packet Type	Type Code
DH1	4_H
DH3	B_H
DH5	F_H

3.12.1.3 Payload

The following figure shows the configuration of the Payload. For CRC, a value that is obtained according to the CRC generation specifications, which are prescribed in section 7.1.2 of BLUETOOTH SPECIFICATION Version 2.0 + EDR[vol3], is assigned with UAP = 00_H.

Payload

LLID	FLOW	LENGTH	UNDEFINED	PAYLOAD BODY	CRC

LLID:	Logical link indication	2_H (2 bits)
FLOW:	Flow indication	1_H (1 bit)
LENGTH:	payload length indicator	See Table 3.12.1.3-1 below.

Table 3.12.1.3-1 LENGTH for BR

Packet Type	Data Length	Value
DH1	5 bits	27
DH3	9 bits	183
DH5	9 bits	339

3.12.2 Packet configuration for Enhanced Data Rate (EDR)

When a waveform pattern of 2-DH1, 2-DH3, 2-DH5, 3-DH1, 3-DH3, 3-DH5, 2-DH3_3SlotOff, 2-DH5_5SlotOff, 3-DH3_3SlotOff, or 3-DH5_5SlotOff is selected, the data is output in the format shown in Figure 3.12.2-1 below. Table 3.12.2-1 shows the payload body data length for each file.

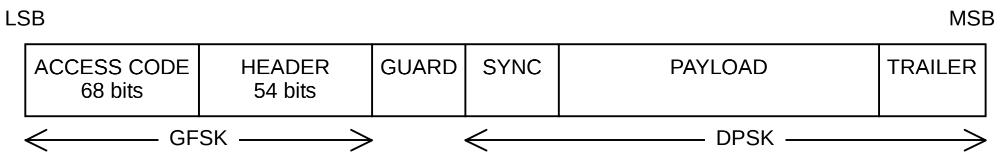


Figure 3.12.2-1 Packet configuration for Enhanced Data Rate waveform

Table 3.12.2-1 Data length of payload body for EDR

Packet Type	Payload Body (Bytes)
2-DH1	54
2-DH3	367
2-DH5	679
3-DH1	83
3-DH3	552
3-DH5	1021

3.12.2.1 ACCESS CODE

The configuration of the ACCESS CODE is the same as that shown in Section 3.12.1.1.

3.12.2.2 Packet Header

The configuration of the Packet Header is the same as that shown in Section 3.12.1.2. Table 3.12.2.2-1 shows the values to be assigned for TYPE (type code).

Table 3.12.2.2-1 Type code (TYPE) for EDR output signal

Packet Type	Type Code
2-DH1	4_H
2-DH3	B_H
2-DH5	F_H
3-DH1	4_H
3-DH3	B_H
3-DH5	F_H

3.12.2.3 Payload

The configuration of the Payload is the same as that shown in Section 3.12.1.3. Table 3.12.2.3-1 shows the data lengths and setting values for LENGTH.

Table 3.12.2.3-1 LENGTH for EDR

Packet Type	Data Length	Value
2-DH1	5 bits	54
2-DH3	10 bits	366
2-DH5	10 bits	678
3-DH1	5 bits	81
3-DH3	10 bits	549
3-DH5	10 bits	1017

3.12.2.4 Synchronous Sequence

The following value is assigned for Synchronous Sequence (SYNC) in each EDR packet. The phase is initialized to 0 rad by setting 0 to the head of Synchronous Sequence.

For 2-DH1, 2-DH3, and 2-DH5 packets: $0777D5_H$ (22 bits)
For 3-DH1, 3-DH3, and 3-DH5 packets: $0175D7E92_H$ (33 bits)

3.12.2.5 Trailer

The following value is assigned for Trailer (TRAILER) in each EDR packet.

For 2-DH1, 2-DH3, and 2-DH5 packets: 0_H (4 bits)
For 3-DH1, 3-DH3, and 3-DH5 packets: 00_H (6 bits)

3.12.3 Packet configuration for BLE

When waveform patterns of BLE, BLE_Dirty, BLE_Dirty_withFM, and BLE_CRC_corrupted of Bluetooth Low Energy (BLE) waveform pattern are selected, the data is output in the format shown in Figure 3.12.3-1. Table 3.12.3-1 shows the payload body data length. The Packet Interval is 1.25 ms.

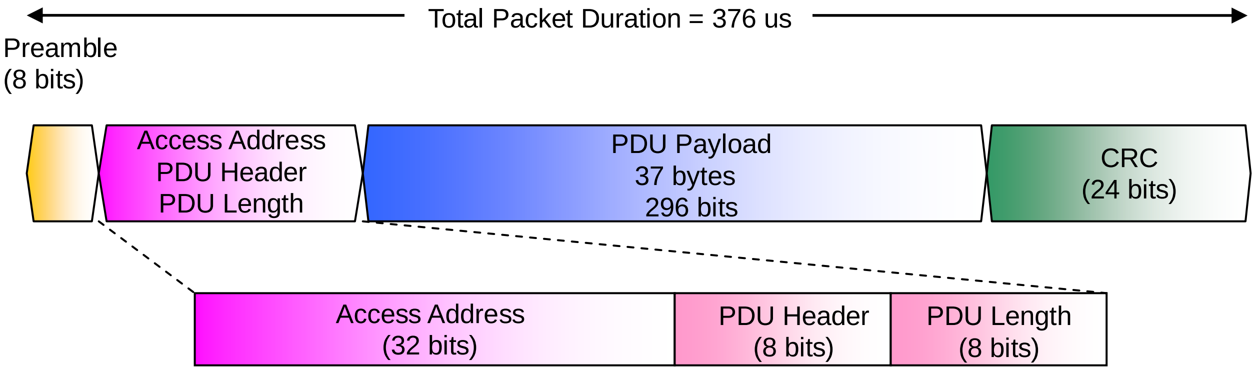


Figure 3.12.3-1 Packet Configuration for BLE Waveform

Table 3.12.3-1 BLE Payload Body Length

Packet type	Payload Body (bytes)
BLE Reference Signal	37

3.12.3.1 Preamble

Preamble is 8 bits of either one of 10101010 or 01010101 depending on LSB of Access Address as specified in Section 2.1.1, BLUETOOTH SPECIFICATION Version 4.0 [vol 6].Because Access Address of BLE, BLE_Dirty, BLE_Dirty_withFM, and BLE_CRC_corrupted is 0x94826E8E$_H$, when LSB of Access Address is 1, the preamble is "10101010" (In this case, the first bit is assumed to be LSB due to the transmission order).

When LSB of Access Address is 1 : 10101010b (8 bits)
When LSB of Access Address is 0 : 01010101b (8 bits)

3.12.3.2 Access Address

Access Address is a bit string of 32 bits as specified in Section 2.1.2, BLUETOOTH SPECIFICATION Version 4.0 [vol 6].Access Address of BLE, BLE_Dirty, BLE_Dirty_withFM, and BLE_CRC_corrupted is 0x94826E8E $_H$.

3.12.3.3 PDU Header, PDU Length

PDU Header and PDU Length are bit strings of 8 bits as specified in Section 2.4, BLUETOOTH SPECIFICATION Version 4.0 [vol 6] and Section 7.2.4, RF-PHY.TS/4.0.0 respectively.

Payload Type (4 bits) '0000'	**'0000'**	**Payload Length in octets (6 bits) '100101'**	**'00'**

PDU Header PDU Length

3.12.3.4 PDU Payload, CRC

PDU Payload is payload data of 6 to 37 bytes as specified in Section 2.4, BLUETOOTH SPECIFICATION Version 4.0 [vol 6].Payload data of BLE, BLE_Dirty, BLE_Dirty_withFM, and BLE_CRC_corrupted is 37 bytes. In addition, CRC is 3 bytes.

3.12.4 Dirty Transmitter Signal

Dirty Transmitter Signal is specified as a signal used for a reception test in Section 5.1.18, Bluetooth Test Specification v1.2/2.0/2.0 + EDR/2.1/2.1 + EDR/3.0/3.0 + HS and Section 6.3.1, RF-PHY.TS/4.0.0. This Dirty Transmitter Signal changes the frequency offset, modulation index, and symbol timing error with every 50 packets. 10 combinations of these three parameters are specified, and outputs of Test Run 1 to 10 are repeated. Furthermore, the frequency drift of output signals is specified for the Dirty Transmitter Signal. The waveform patterns "Dirty" in Table 3.12-1 are waveform patterns with the addition of the frequency offset, modulation index fluctuation, and symbol timing error. In addition, the waveform patterns "Dirty, FM" are signals with the addition of the frequency offset, modulation index fluctuation, symbol timing error, and frequency drift.

3.13 GPS Waveform Pattern

The GPS waveform patterns shown in Table 3.13-1 are provided.

Table 3.13-1 List of GPS waveform patterns

Waveform Pattern Name	Main Usage	Outline of Data
Package name: GPS		
SYNC_ADJ*1	Synchronization adjustment*2	Consists of TLM, HOW, and default navigation data, formatted according to the subframe configuration that is prescribed in GLOBAL POSITIONING SYSTEM STANDARD POSITIONING SERVICE SIGNAL SPECIFICATION. One period is configured with 1 subframes.
TLM*3	Sensitivity test	Consists of TLM, HOW, and default navigation data, formatted according to the subframe configuration that is prescribed in GLOBAL POSITIONING SYSTEM STANDARD POSITIONING SERVICE SIGNAL SPECIFICATION.
PN9	BER measurement	Consecutive PN9 data, not configured in a subframe format
PARITY	Parity detection	Configured in the Word format that is prescribed in GLOBAL POSITIONING SYSTEM STANDARD POSITIONING SERVICE SIGNAL SPECIFICATION. One Word consists of 24-bit PN9fix data and 6-bit parity bit data.
TLM_PARITY *4	Sensitivity test	Consists of TLM, HOW, and Nav Data, formatted according to the subframe configuration that is prescribed in GLOBAL POSITIONING SYSTEM STANDARD POSITIONING SERVICE SIGNAL SPECIFICATION. Random data is inserted into the Nav Data part of Word3 to Word10. One period is configured with 5 subframes.
Data0, Data1, Data10, Data1C	Synchronization adjustment	Used in combination with SYNC_ADJ. These waveform patterns are automatically loaded into the memory when SYNC_ADJ is loaded into the memory. Users do not have to perform loading and selecting of these waveform patterns, because these waveform patterns are automatically selected when SYNC_ADJ is selected.

*1: When using SYNC_ADJ, press the Baseband key on the MG3710A and set Pattern Combination to Defined. Refer to the MG3710A Vector Signal Generator Operation Manual (Mainframe) for details on how to configure the settings.

*2: The repeatability of the subframe output timing of RF output against an external start trigger input is reduced to 10 ns or less.

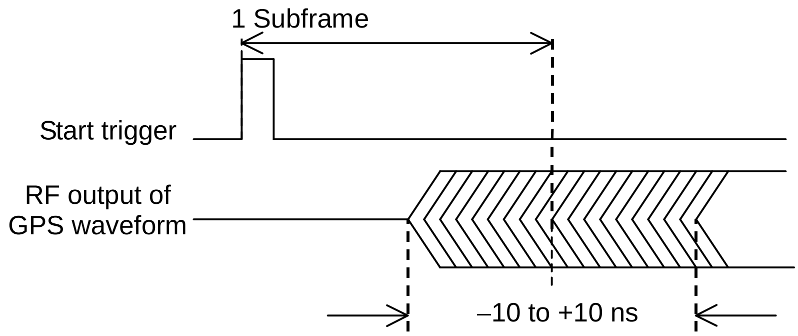


Figure 3.13-1 SYNC_ADJ output timing

*3: When executing a Doppler test, change the RF frequency and sampling clock at the same rate.
The sampling clock when the Doppler frequency is 0 Hz is 4.092 MHz. For example, when applying a +4-kHz Doppler frequency, the following expression establishes (providing the sampling clock as "CLK"):

(1575.42 MHz + 4 kHz)/1575.42 MHz = CLK/4.092 MHz
then;
CLK = 4.09201039 MHz

Refer to *MG3710A Operation Manual (Mainframe)* for RF frequency and sampling clock settings.

*4: To use this waveform pattern, Combination of Baseband Signal (option), ARB Memory Upgrade 256 Msample (option), or ARB Memory Upgrade 1024 Msample (option), is required.

When outputting each TLM and PARITY waveform pattern, marker signal (Marker 1, Marker 2) as outlined in the Table 3.13-2 is output from Marker1 Output connector of MG3710A rear panel or from AUX connector. For details of output connector setting, refer to 7.4.2 "Route Output Connectors" in MG3710A Vector Signal Generator Operation Manual (Mainframe).

Table 3.13-2 Marker output data and IQ output level

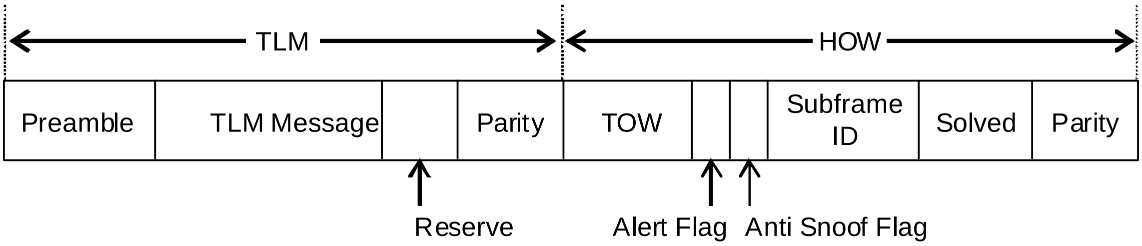
Marker Signal	Output Data
Marker 1	Packet Clock
Marker 2	RF Gate
Marker 3	–

3.13.1 Waveform format

The following figures show the formats of the waveforms listed in Table 3.13-1 above. Each data is spread by the C/A code with Satellite ID Number 1. See Figure 3.13.1-1 for the C/A code generation.

SYNC_ADJ, TLM

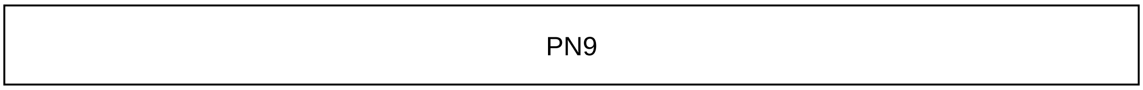
TLM:	Telemetry	30 bits
HOW:	Handover word	30 bits
Data:	Default navigation data	240 bits



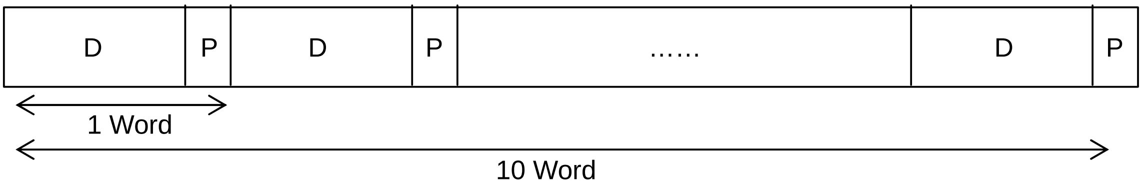
Preamble:	$8B_H$ (8 bits)
TLM message:	00_H (14 bits)
Reserved:	3_H (2 bits)
TOW (Time of Week):	00000_H (17 bits)
Alert flag:	0_H (1 bit)
Anti snoof flag:	0_H (1 bit)
Subframe ID:	1_H (3 bits)
Solved:	1_H (2 bits)
Parity Bit:	Parity Bit (6 bits)

Figure 3.13.1-1 Waveform format of GPS

PN9



PARITY

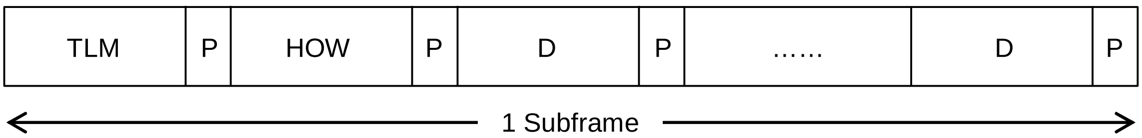


D:	Data	24 bits
P:	Parity bit	6 bits

PN9fix data is allocated to the Data part. Adjacent Word PN data is contiguous but the PN data is discontiguous at the 10th Word and the 1st Word of the next cycle.

Figure 3.13.1-2 Waveform format of GPS_PN9, PARITY

TLM_PARITY



TML:	Telemetry	24 bits
HOW:	Handover word	24 bits
D:	Data	24 bits
P:	Parity bit	6 bits

Random data is assigned to Data parts.

Figure 3.13.1-3 Waveform format of GPS TLM_PARITY

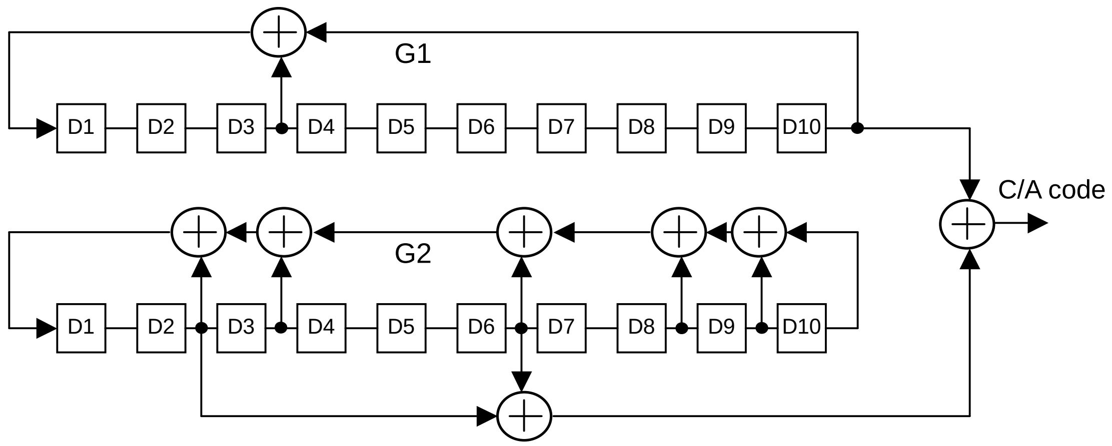


Figure 3.13.1-4 C/A code generation

3.14 Mobile WiMAX Waveform Pattern

The Mobile WiMAX patterns shown below are provided as Mobile WiMAX waveform patterns.

Table 3.14-1 Mobile WiMAX Waveform Patterns

Waveform Pattern Name	Main Use	Data Summary
Package name: Mobile WiMAX		
WiMAX_DL_10MHz_QPSK	BS TX Device Test	Includes Preamble, FCH, and DL-MAP Modulation method is QPSK DL-Burst mapped waveform pattern
WiMAX_DL_10MHz_64QAM		Includes Preamble, FCH, and DL-MAP Modulation method is 64QAM BL-Burst mapped waveform pattern

3.14.1 Waveform format

WiMAX_DL_10MHz_QPSK

The parameters for this waveform pattern are listed in the following table. The channel-coded data corresponding to the PN9Fix data is mapped at DL-Burst.

Table 3.14.1-1 Waveform Pattern Parameters (WiMAX_DL_10MHz_QPSK)

Parameter	Settings
Bandwidth	10 MHZ
Frame Duration	5 ms
Preamble Index	0
Number of OFDMA Symbols	31 symbols (Including Preamble)
FCH	Yes
DL-MAP	Yes
DL-Burst FEC Type	CTC (1/2)
DL-Burst Modulation Method	QPSK

The frame composition is shown below.

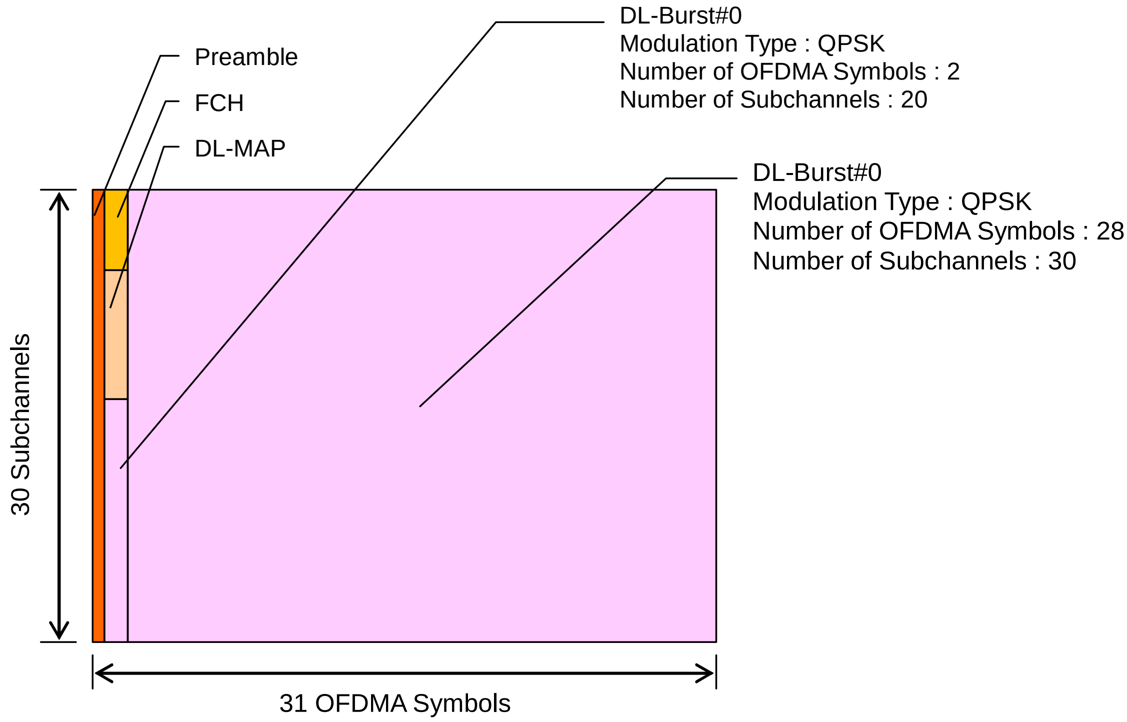


Figure 3.14.1-1 WiMAX_DL_10MHz_QPSK Frame Composition

WiMAX_DL_10MHz_64QAM

The parameters for this waveform pattern are listed in the following table. The channel-coded data corresponding to the PN9Fix data is mapped at DL-Burst.

Table 3.14.1-2 Waveform Pattern Parameters (WiMAX_DL_10MHz_64QAM)

Parameter	Settings
Bandwidth	10 MHZ
Frame Duration	5 ms
Preamble Index	0
Number of OFDMA Symbols	31 symbols (Including Preamble)
FCH	Yes
DL-MAP	Yes
DL-Burst FEC Type	CTC (1/2)
DL-Burst Modulation Method	64QAM

The frame composition is shown below.

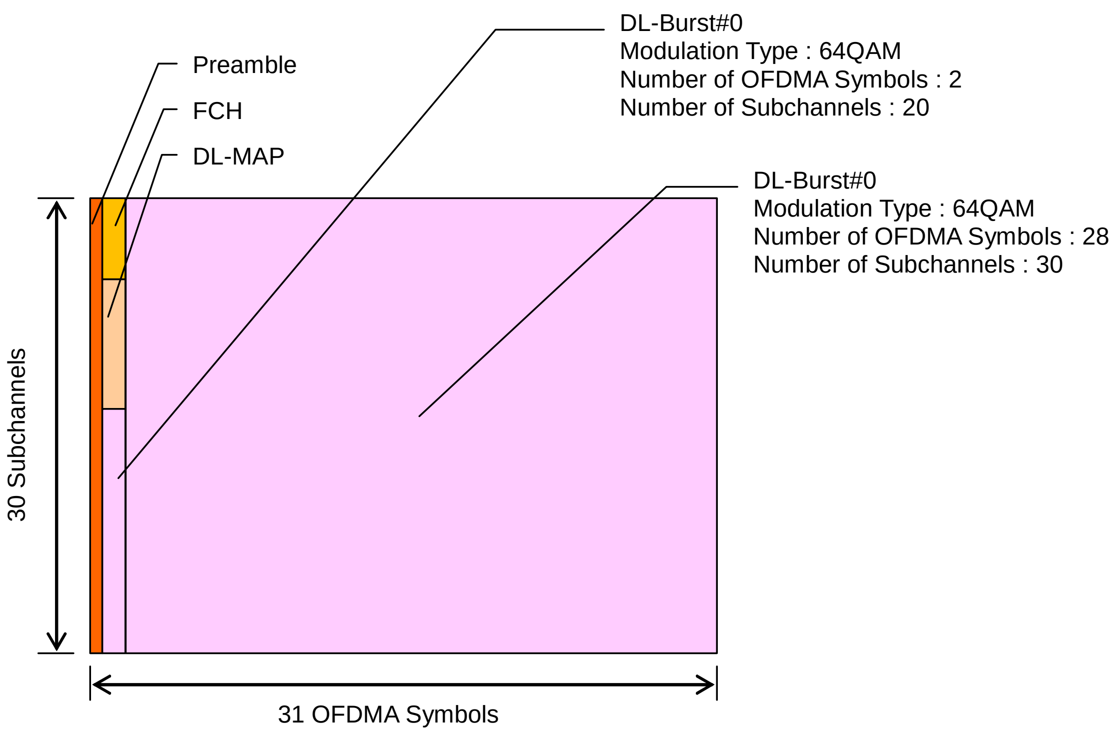


Figure 3.14.1-2 WiMAX_DL_10MHz_64QAM Frame Composition

3.15 Tone Signal Waveform Pattern

The following table lists the waveform patterns and combination file that are available as tone signal waveform pattern.

Table 3.15-1 Tone Signal Waveform Pattern

Waveform Pattern Name	Main Use	Data Summary
Package name: Tone		
+1MHz_Tone	Device Test	Tone signal with +1 MHz frequency offset
–1MHz_Tone		Tone signal with –1 MHz frequency offset
DC_Tone		Tone signal without any frequency offset

Table 3.15-2 Tone Signal Combination File

Waveform Pattern Name	Main Use	Data Summary
Package name: Tone		
2Tones_+1MHz_–1MHz	Device Test	Signal that combines tone signal with +1 MHz frequency offset and tone signal with –1 MHz frequency offset.

Note:

To use this combination file, Combination of Baseband Signal (option) is required.

3.16 Waveform Pattern for Phase Adjustment

The following table lists the waveform patterns that are available for MG3710A's phase adjustment.

Table 3.16-1 Waveform Pattern for Phase Adjustment

Waveform Pattern Name	Main Use	Data Summary
Package name: PhaseCoherence		
Adjustment	For phase adjustment of MG3710A	This is used to adjust phase and timing when outputting MIMO signal from MG3710A.

3.17 GLONASS Waveform Pattern

The GLONASS waveform patterns shown in Table 3.17-1 are provided.

Table 3.17-1 GLONASS waveform patterns

Waveform Pattern Name	Main Use	Data Summary
Package name: GLONASS		
15String _PN9	Sensitivity test Check bit Detection	It has String Navigation bit structure specified in GLOBAL NAVIGATION SATELLITE SYSTEM INTERFACE CONTROL DOCUMENT.
15String _Message	Sensitivity test Check bit Detection	It has String Navigation bit structure specified in GLOBAL NAVIGATION SATELLITE SYSTEM INTERFACE CONTROL DOCUMENT.
GLONASS_PN9	BER measurement	Consecutive PN9 data, not configured in a String, Frame format

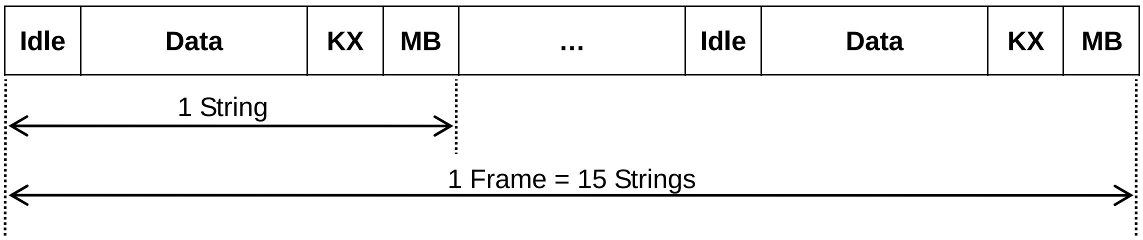
When outputting each 15String _PN9 and 15String _Message waveform pattern, marker signal (Marker 1, Marker 2) as outlined in the Table 3.17-2 is output from Marker1 Output connector of MG3710A rear panel or from AUX connector. For details of output connector setting, refer to 7.4.2 “Route Output Connectors” in MG3710A Vector Signal Generator Operation Manual (Mainframe).

Table 3.17-2 Marker output data and IQ output level

Marker Signal	Output Data
Marker1	Frame Clock
Marker2	String Clock
Marker3	——

3.17.1 Waveform format

The following figures show the formats of the waveforms listed in Table 3.17-1 above.



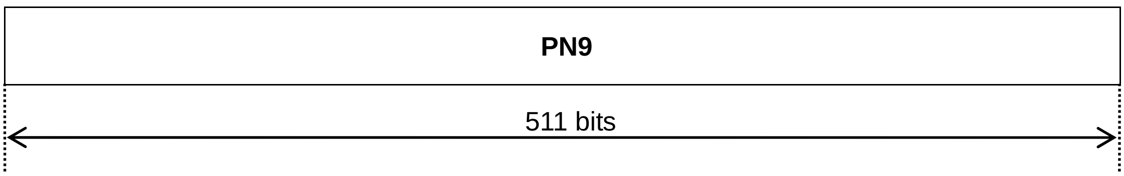
Idle:	Idle chip	1 bit	[50 bps]
Data:	Random data*[1]	76 bits	[50 bps]
KX:	Check bit	8 bits	[50 bps]
MB:	Time Mark*[2]	30 bits	[100 bps]

*1: PN9fix or Random data is assigned to Data parts.
Data is discontinuous, for it is reset every 1 frame.

*2: Generator polynomial of Time Mark

$$g(x) = 1 + x^3 + x^5$$

Figure 3.17.1-1 Waveform format of 15String _PN9 and 15String _Message



PN9:	PN9 data	511 bits	[100 bps]

Figure 3.17.1-2 Waveform format of GLONASS_PN9

3.18 QZSS Waveform Pattern

The QZSS waveform patterns shown in Table 3.18-1 are provided.

Table 3.18-1 List of QZSS waveform patterns

Waveform Pattern Name	Main Use	Data Summary
Package name: QZSS		
DefaultNavData	Sensitivity test	Consists of TLM, HOW, and default navigation data, formatted according to the subframe configuration that is prescribed in GLOBAL POSITIONING SYSTEM STANDARD POSITIONING SERVICE SIGNAL SPECIFICATION.
PARITY	Parity detection	Configured in the Word format that is prescribed in GLOBAL POSITIONING SYSTEM STANDARD POSITIONING SERVICE SIGNAL SPECIFICATION. One Word consists of 24-bit PN9fix data and 6-bit parity bit data.
ENC	Parity detection	Configured in the Word format that is prescribed in GLOBAL POSITIONING SYSTEM STANDARD POSITIONING SERVICE SIGNAL SPECIFICATION. One Word consists of 24-bit Random data and 6-bit parity bit data.
QZSS_PN9	BER measurement	Consecutive PN9 data, not configured in a subframe format

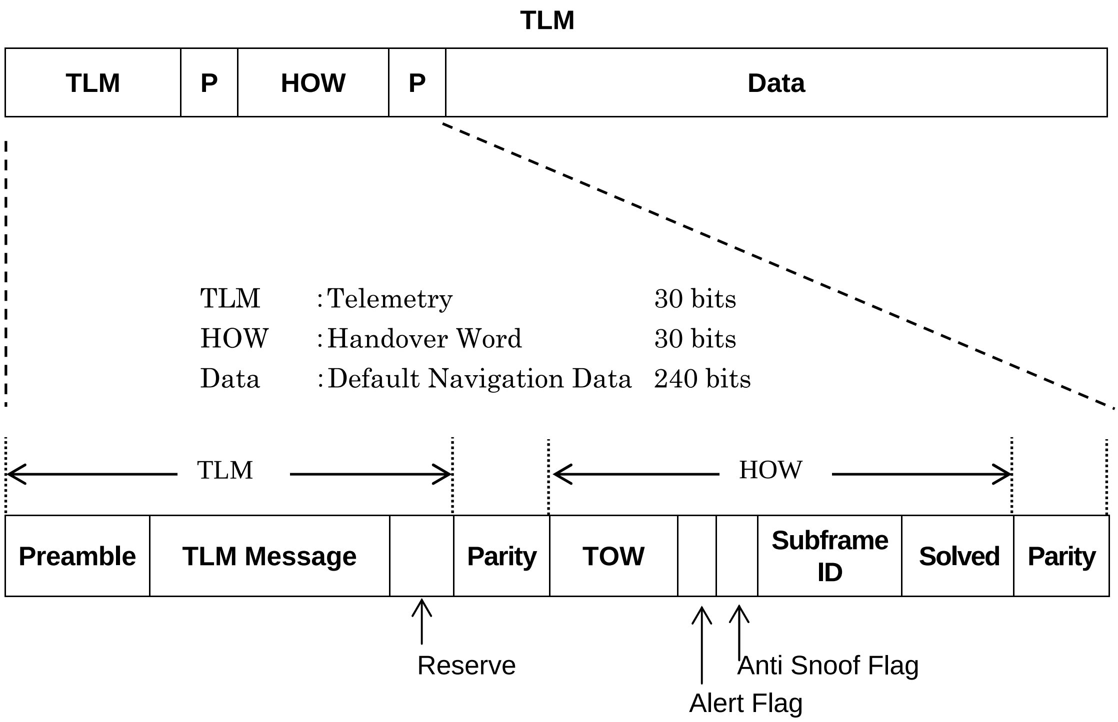
When outputting each DefaultNavData, PARITY and ENC waveform pattern, marker signal (Marker 1, Marker 2) as outlined in the Table 3.18-2 is output from Marker1 Output connector of MG3710A rear panel or from AUX connector. For details of output connector setting, refer to 7.4.2 “Route Output Connectors” in MG3710A Vector Signal Generator Operation Manual (Mainframe).

Table 3.18-2 Marker output data and IQ output level

Marker Signal	Output Data
Marker1	Subframe Clock
Marker2	RF Gate
Marker3	——

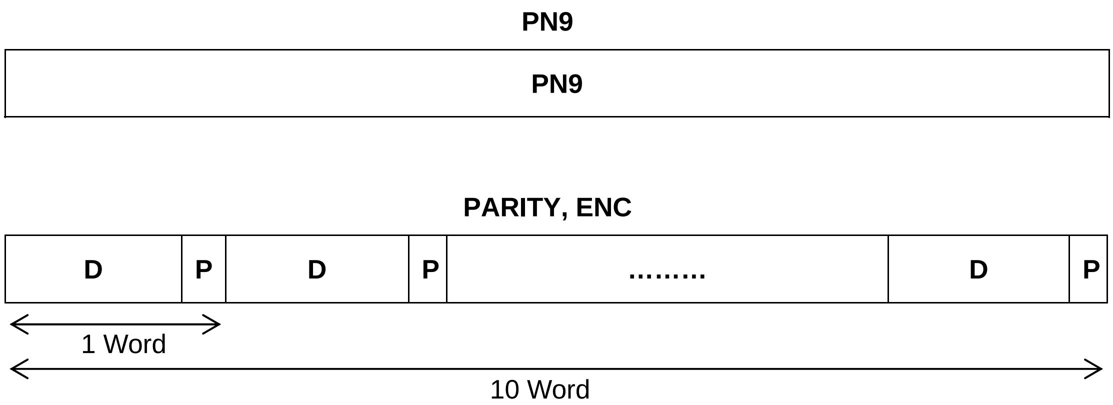
3.18.1 Waveform format

The following figures show the formats of the waveforms listed in Table 3.18-1 above. Each data is spread by the C/A code with Satellite ID Number 193. See Figure 3.18.1-1 for the C/A code generation.



Preamble:	$8B_H$ (8 bits)
TLM Message:	00_H (14 bits)
Reserved:	3_H (2 bits)
TOW (Time of Week):	00000_H (17 bits)
Alert Flag:	0_H (1 bit)
Anti Snoof Flag:	0_H (1 bit)
Subframe ID:	1_H (3 bits)
Solved:	1_H (2 bits)
Parity Bit:	Parity Bit (6 bits)

Figure 3.18.1-1 Waveform format of DefaultNavData



D :Data 24 bits
P :Parity Bit 6 bits
PN9fix data is allocated to the Data part. Adjacent Word PN data is contiguous but the PN data is discontiguous at the 10th Word and the 1st Word of the next cycle in PARITY waveform.

Figure 3.18.1-2 Waveform format of QZSS_PN9, PARITY, ENC

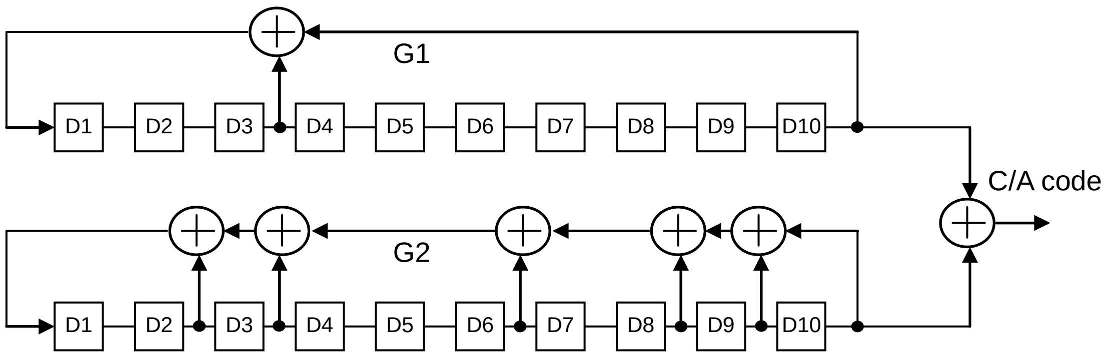


Figure 3.18.1-3 C/A code generation

3.19 Interference Waveform Pattern

Table 3.19-1 shows the interference waveform patterns provided for receiving performance test.

Table 3.19-1 List of interference waveform patterns

System Name	Combination File Name (Package Name)	Waveform Name (Package Name)	File Type	Data Summary
W-CDMA Downlink	W-CDMA_DL_Interferer (Interferer)*	DL_Interferer_ov3 (W-CDMA_A(UE Rx test))	Combination File	Interferer defined in 3GPP TS34.121-1 E.4. Refer to 3.1.6 "DL_Interferer" in this operation manual.
LTE FDD Downlink	-	FDD_DL_xxMx_Interfer (Interferer)	Waveform Pattern	Waveform pattern defined in 3GPP TS36.521-1 Table A3.2-1.xxMx represents channel bandwidth.
LTE TDD Downlink	-	TDD_DL_xxMx_Interfer (Interferer)	Waveform Pattern	Waveform pattern defined in 3GPP TS36.521-2 Table A3.2-2.xxMx represents channel bandwidth.
GSM	GSM_Interferer (Interferer)*	GMSK_PN9 (GSM)	Combination File	Refer to the description about GMSK_PN9 in Chapter 3.7 of this operation manual.
TD-SCDMA	-	TD-SCDMA_Interferer (Interferer)	Waveform Pattern	Interferer defined in Chapter 6 of 3GPP TS34.122. Continuous wave of chip rate =1.28M/s, 1 code, and roll off rate =0.22.

*: Output is enabled by calling an interferer package combination file (alias) or a direct waveform pattern. The combination files in this table are set to alias. Alias is a function to call a waveform pattern from a different package such as a shortcut file.

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